國立雲林科技大學
94學年度碩士班入學招生考試試題

系所：電子系
科目：電子學

計算題共六題

1. For the circuit shown in Fig. p1,

(1)(3%) find the transfer function $T(s)=\frac{V_o(s)}{V_i(s)}$.

(2) (3%) Is this a high-pass or a low-pass network?

(3) (3%) What is its transmission at very high frequencies?

(4) (3%) What is the corner frequency ω_0?

(5) (3%) For $R_1=10k\Omega$, $R_2=20k\Omega$, and $C=1\mu F$, find f_0?

(6) (3%) What is the value of $|T(j\omega_0)|$?

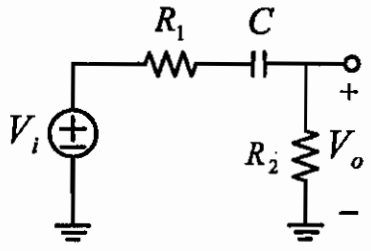

Fig. p1.

2. (20%)A CMOS switch is used to connect a sinusoidal source $0.1\sin\omega t$ to a load capacitance C. For ± 5V control signals and $k_n'(\frac{W}{L})_n=k_p'(\frac{W}{L})_p=100\mu A/V^2$, $V_{tn}=|V_{tp}|=1V$, what is the cut-off frequency introduced by the switch if C=1000pF?

3. (12%) Consider an ideal voltage amplifier with a gain of 0.95V/V and a resistance R=100kΩ connected in the feedback path-that is, between the output and input terminals. Use Miller's theorem to find the input resistance of this circuit.

4. Fig.p4 shows an oscillator circuit of the Colpitts type. Base on this circuit, answer the following questions:
   (1) (5%) Sketch the small signal model.
   (2) (5%) Derive an equation governing circuit operation.
   (3) (10%) Find the frequency of oscillation and the gain condition that ensures that oscillations start.

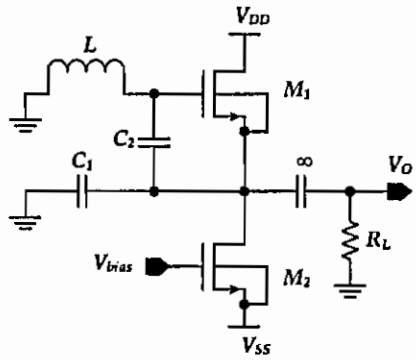

Fig.p4

5. A MOSFET is specified to have maximum power dissipation P_D of 5 watts at an ambient temperature T_A of 25°C, and the maximum junction temperature T_{Jmax} of 200°C.
   (1) (5%) Find the thermal resistance θ_{JA}.
   (2) (10%) Assume the thermal resistance between junction and heat sink is 2 °C/W, and the ambient temperature is 45 °C. Find two case-to-ambient thermal resistances for this MOSFET working safely in junction temperatures of 85 °C and 125 °C, respectively.

6. (15%) A shunt-series feedback amplifier shown in Fig.p6, and using an ideal basic current amplifier operates with $I_S = 20$ μA, $I_f = 18$ μA and $I_O = 6$ mA. What are the values of A and β which correspond? Include the correct units for each.

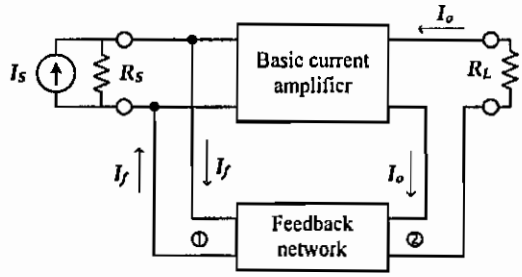

Fig.p6

國立雲林科技大學
94學年度碩士班入學招生考試試題

系所：電子系
科目：微電子學

本試卷共有六大題，總分爲 100 分

1. Determine the electron and hole concentrations in a silicon sample at room temperature containing 5.0×10^{16} phosphorus atoms/cm^3 and 2.0×10^{15} boron atoms/cm^3. **(15%)**

2. Explain the Early effect in an npn bipolar junction transistor (BJT). **(15%)**

3. Sketch the circuit configuration of a CMOS switch and explain its operation. **(20%)**

4. Sketch the circuit connections and give the relation between the output voltage, V_o, and input voltage , V_i, in terms of the circuit elements, for the following circuits of the op-amp. **(20%)**
   (a) Inverting Amplifier
   (b) Summing Amplifier
   (c) Integrator
   (d) Unity Follower

5. For the circuit of Fig.1, calculate (a) the input power, (b) output power, and (c) power handled by each output transistor and (d) the circuit efficiency for an input of 12 V rms. **(16%)**

6. Describe the operation of the circuit of Fig.2. and also express the output V_o as a function of V_i. **(14%)**

國立雲林科技大學
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系所：電子系
科目：微電子學

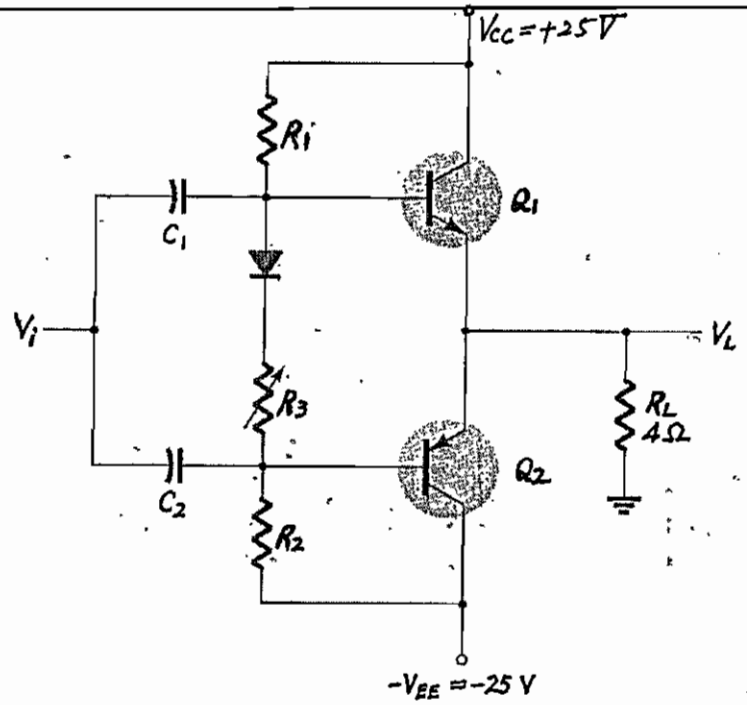

Fig.1.

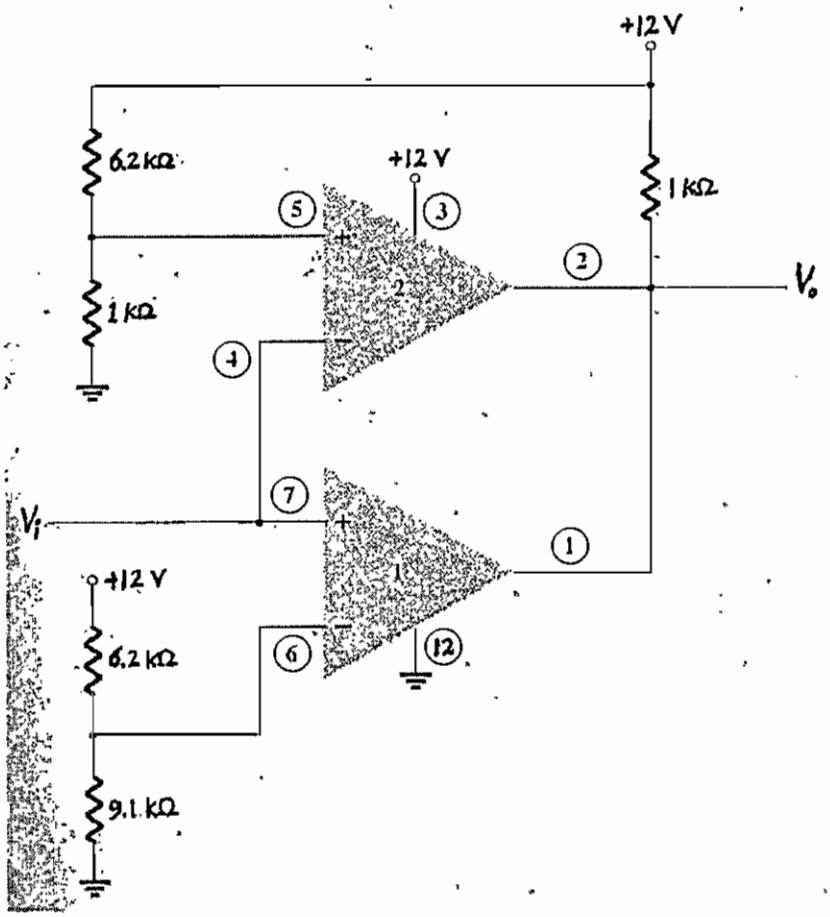

Fig.2.

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94學年度碩士班入學招生考試試題

系所：電子系
科目：積體電路設計

1. (20 pts) Please reorder the VLSI design flow and specify its EDA tools as the following terms
   a) Reorder the Cell-Based design flow (6 pts)
      Specification → RTL Design & Synthesis → Post-layout Simulation → Placement & Routing → Behavior Design → Gate-level Simulation → RC Extraction → IC Tape Out
   b) Specify any one EDA tool for the Cell-Based design flow (6 pts)
      1. RTL Synthesis
      2. Post-layout Simulation
      3. Placement & Routing
      4. Behavior Design
      5. Gate-level Simulation
      6. RC Extraction
   c) Reorder the Full-Custom design flow (4 pts)
      Circuit Level Design → Physical Verification and RC Extraction → Post-layout Circuit Simulation → Physical Layout → Pre-layout Circuit Simulation → IC Tape Out
   d) Specify any one EDA tool for the Full-Custom design flow (4 pts)
      1. Circuit-level Design Entry
      2. Physical Verification and RC Extraction
      3. Post-layout Circuit Simulation
      4. Physical Layout

2. (15pts) The SOP expression of a 4:1 multiplexor is specified as the following

   $$f = p_0 \cdot \overline{s_1} \cdot \overline{s_0} + p_1 \cdot \overline{s_1} \cdot s_0 + p_2 \cdot s_1 \cdot \overline{s_0} + p_3 \cdot s_1 \cdot s_0$$

   a) Please draw the logic diagram of the 4:1 multiplexor f using the INVETER and NAND gates only (5 pts)
   b) Please design the 4:1 multiplexor f using nFET (nMOS) pass transistors (5 pts)
   c) Please design the 4:1 multiplexor f using split-array nFET (nMOS) and pFET (pMOS) for full-rail swing output (5 pts)

3. (15pts) Static random-access memory (SRAM) design
   a) Please draw the 4-transistor 1-bit SRAM cell circuit schematic (5 pts)
   b) Please draw the 6-transistor 1-bit SRAM cell circuit schematic (5 pts)
   c) Please draw the 2-port 6-transistor 1-bit SRAM cell circuit schematic (5 pts)

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系所：電子系
科目：積體電路設計

4. a) In order to drive a large capacitance (C_L= 20 pF) from a minimum size gate (with input capacitance C_i=10 fF), you decide to introduce a two-staged buffer as shown in Figure 1. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay. (5pts)

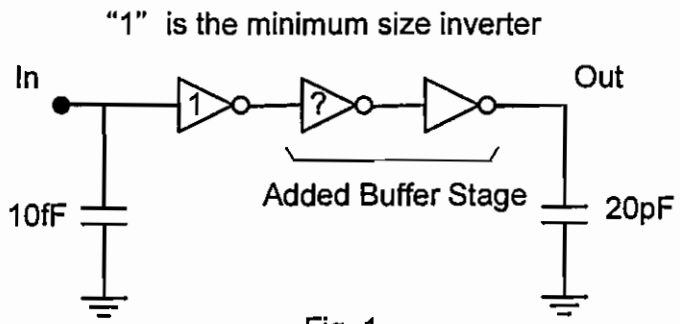

Fig. 1

b) If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case? (6 pts)

c) Determine the power consumption of the circuit designed by (a) in working frequency 250MHz. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V and an activity factor of 1? (6 pts)

5. Please design the following logic styles: (a) pass-transistor logic, (b) differential cascade voltage switch logic (DCVSL), (c) complementary CMOS gate, (d) pseudo NMOS, (e) dynamic logic, such that these gates can implement the Boolean function $S = ABC + A\overline{BC} + \overline{A}BC + \overline{A}B\overline{C}$. Assume A, B, C, and their complements are available as input. (15 pts)

6. Consider the circuit in Figure 2. The inverter is ideal, with $V_M=V_{DD}/2$ and infinite slop. The transistors have $V_{Tn} = |V_{Tp}| = 0.4V$, $k_n' = 120\mu A/V^2$, $k_p' = -40\mu A/V^2$. M_1 has $(W/L)_1$=1. Ignore all other parasitic effects in the transistors.,

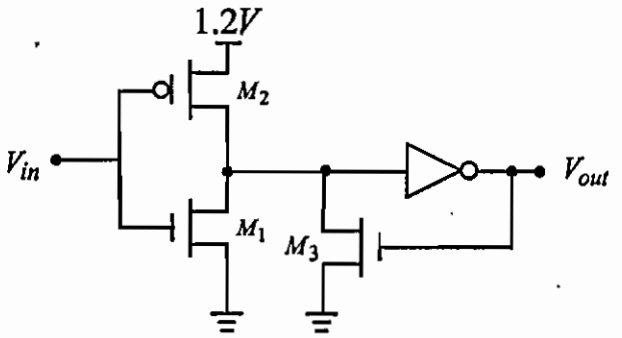

Fig. 2

a) As V_{in} goes from 0 to V_{DD} and back to 0 explain the sequence of events which makes this circuit operate as a Schmitt Trigger. (6 pts)

b) Find the value of $(W/L)_2$ such that when V_{in} increases from 0 to V_{DD} the output will switch at V_{in}=0.8V. (6 pts)

c) If you use $(W/L)_2$=5, please find the value of $(W/L)_3$ such that when V_{in} decreases from V_{DD} to 0 the output will switch at V_{in}=0.4V. (6 pts)

國立雲林科技大學
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系所：電子系
科目：計算機組織

1. (5 points)(a)Explain what a decoder circuit does. Be sure to state how many input and output lines it has.
(b)If 00010000 is the output from a decoder, what was the input? (Assume that the output digits are numbered from right to left).

2. (5 points) Consider the following structure of the instruction register.

Op code	Address-1	Address-2
6 bits	18 bits	18 bits

(a) What is the maximum number of distinct operation codes that can be recognized and executed by the processor on this machine?
(b)What is the maximum memory size on this machine?

3. (10 points) Consider the following fragment of C code:

```
for (i=0; i<=100; i++)
   a[i] = b[i] +c;
```

Assume that a and b are arrays of words and the base address of a is in $a0 and the base address of b is in $a1. Register $t0 is associated with variable i and register $s0 with the value of c. Write the code for MIPS. How many instructions are executed during the running of this code if there are no array out-of-bounds exceptions thrown? How many memory data references will be made during execution?

4. (10 points) Show the layout of a cache for a CPU that can address 1M*16 of memory; the cache holds 8K*16 of data and has the following mapping strategies. Please give the number of bits per location and the total number of locations.
(a) Fully associative
(b) Direct mapped
(c) Two-way set associative
(d) Four-way set associative

5. (10 points) An instruction pipeline has five stages with propagation delays of 20ns, 25ns, 20ns, 70ns, and 40 ns, respectively.
(a) What is the clock period of the pipeline?
(b) How much time does the pipeline need to complete 100 instructions?
(c) What is the speedup of the pipeline?

6. (10 points) Assume that a two-address machine, the operation code is stored in location 200 and the address field is stored in location 201 with value 400. There is a register R1 with value 200. What is the effective address by (a)direct addressing, (b)immediate addressing, (c)PC-relative addressing, and (d) register indirect addressing.

7. (10 points) The pipeline of the Fig.1 has the propagation times: 35 ns for the operands to be read from memory into registers R1, R2 and R4, 35 ns for the signal to propagate through the multiplier, 5 ns for the transfer into R3, and 25ns to add the two numbers, and 5 ns for the transfer into R5. What is the minimum clock cycle time that can be used for this circuit?

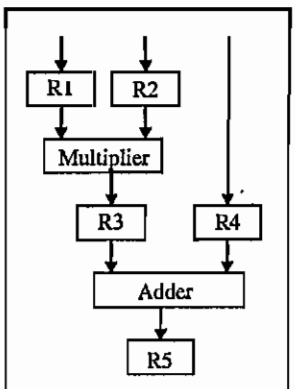

Figure 1

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系所：電子系
科目：計算機組織

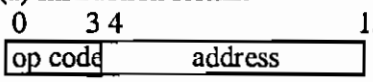
8. (10 points) The number of clock cycles for each instruction class is the following: loads: 6, stores: 5, ALU instructions: 5, Branches: 4, and Jumps:4. Assume the gcc instruction mix is 25% loads, 10% stores, 20% branches, 5% jumps, and 40% ALU. What is the CPI?

9. Once we write the value 0x12345678H to the memory address 0x2000,
   (a) (5 points) For a big-endian CPU, what is the value of memory address 0x2003?
   (b) (5 points) For a little-endian CPU, what is the value of memory address 0x2002?

10. Figure 2 shows the information about the instruction format, integer format, internal CPU registers and the partial list of Opcodes. Figure 3 shows the detail values about the memory and the associated CPU registers. when the CPU executes the program from memory 300h to memory 304h (the instruction of memory address 304h have been exccuted),
   (a) (5 points) What is the value of the memory address 940h?
   (b) (5 points) What is the value of the memory address 941h?

Figure 2

(a) Instruction format



(b) Integer format

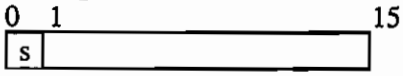
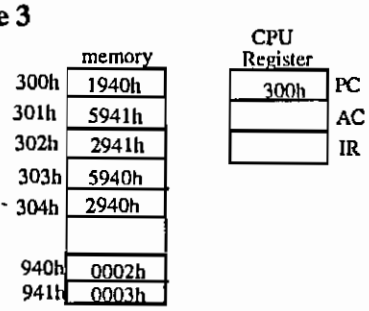


Figure 3



(c) Internal CPU Registers
- Program Counter (PC) = Address of Instruction
- Instruction Register (IR) = Instruction Being Executed
- Accumulator (AC) = Temporary Storage

(d) Partial List of Opcodes
- 0001 = load AC from memory
- 0010 = store AC to memory
- 0101 = add to AC from memory

11. (5 points) (a)We assume that some one-bit full adder will consume 2 ns to derive SUM value and 2 ns to derive the CARRY value. If we use this one-bit full adder to construct 5-bit full adder, what is the maximum working frequency for this 5-bit full adder?

    (5 points) (b)Assume the working frequency of a CPU is 60 MHz. And each instruction spends averagely 3 clocks cycle. How many MIPSs of the CPU?

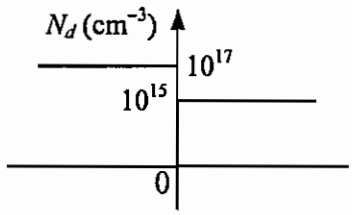
國立雲林科技大學
94 學年度碩士班入學招生考試試題

系所：電子系、光電所
科目：半導體元件

1. Calculate the ionization energy and radius of the donor electron in silicon using the Bohr theory. (20%)

2. A silicon Hall device at $T = 300$ K has the following geometry: d = 10^{-3} cm, W= 10^{-2} cm and L= 10^{-1} cm. The following parameters are measured; $I_x = 0.75$ mA, $V_x = 15$ volts, $V_H = +5.8$ mV, and $B_z = 1000$ guass = 10^{-1} Tesla. (20%)
   Determine (a) the conductivity type. (5%)
   (b) the majority carrier concentration (7%)
   and (c) the majority carrier mobility. (8%).

3. The doping profile of an n-n isotype step junction is shown in the figure. Determine the built-in potential barrier. (14%)



4. Explain the following non-ideal effects in a bipolar transistor: (a) base width modulation, and (b) current crowding. (16%)

5. The metalurgical base width of a silicon npn bipolar transistor is $W_B = 0.6$ μm. The base and collector doping concentrations are $N_B = 3 \times 10^{16}$ cm^{-3} and $N_C = 10^{15}$ cm^{-3}. Neglecting the space charge width of the B-E junction, find the punch-through breakdown voltage at the B-C junction. (15%)

6. An ideal n-channel MOSFET has an inversion carrier mobility $\mu_n = 525$ cm^2/V·s, a threshold voltage $V_T = +0.53$ V, and an oxide thickness $t_{ox} = 100$Å. When biased in the saturation region, the required rated current is I_D(sat) = 5 mA when $V_{GS} = 3$ V. Determined the required W/L ratio. $T = 300$ K. (15%).

Table B.4 | Silicon, gallium arsenide, and germanium properties ($T = 300$ K)

Property	Si	GaAs	Ge
Atoms (cm^{-3})	5.0×10^{22}	4.42×10^{22}	4.42×10^{22}
Atomic weight	28.09	144.63	72.60
Crystal structure	Diamond	Zincblende	Diamond
Density (g/cm^{-3})	2.33	5.32	5.33
Lattice constant (Å)	5.43	5.65	5.65
Melting point (°C)	1415	1238	937
Dielectric constant	11.7	13.1	16.0
Bandgap energy (eV)	1.12	1.42	0.66
Electron affinity, χ (volts)	4.01	4.07	4.13
Effective density of states in conduction band, N_c (cm^{-3})	2.8×10^{19}	4.7×10^{17}	1.04×10^{19}
Effective density of states in valence band, N_v (cm^{-3})	1.04×10^{19}	7.0×10^{18}	6.0×10^{18}
Intrinsic carrier concentration (cm^{-3})	1.5×10^{10}	1.8×10^{6}	2.4×10^{13}
Mobility ($cm^2/V\text{-}s$)			
Electron, μ_n	1350	8500	3900
Hole, μ_p	480	400	1900
Effective mass $\left(\frac{m^*}{m_0}\right)$			
Electrons	$m_l^* = 0.98$	0.067	1.64
	$m_t^* = 0.19$		0.082
Holes	$m_{lh}^* = 0.16$	0.082	0.044
	$m_{hh}^* = 0.49$	0.45	0.28
Effective mass (density of states)			
Electrons $\left(\frac{m_n^*}{m_0}\right)$	1.08	0.067	0.55
Holes $\left(\frac{m_p^*}{m_0}\right)$	0.56	0.48	0.37

Table B.3 | Physical constants

Avogadro's number	$N_A = 6.02 \times 10^{+23}$ atoms per gram molecular weight
Boltzmann's constant	$k = 1.38 \times 10^{-23}$ J/K $= 8.62 \times 10^{-5}$ eV/K
Electronic charge (magnitude)	$e = 1.60 \times 10^{-19}$ C
Free electron rest mass	$m_0 = 9.11 \times 10^{-31}$ kg
Permeability of free space	$\mu_0 = 4\pi \times 10^{-7}$ H/m
Permittivity of free space	$\epsilon_0 = 8.85 \times 10^{-14}$ F/cm $= 8.85 \times 10^{-12}$ F/m
Planck's constant	$h = 6.625 \times 10^{-34}$ J-s $= 4.135 \times 10^{-15}$ eV-s $\frac{h}{2\pi} = \hbar = 1.054 \times 10^{-34}$ J-s
Proton rest mass	$M = 1.67 \times 10^{-27}$ kg
Speed of light in vacuum	$c = 2.998 \times 10^{10}$ cm/s
Thermal voltage ($T = 300$ K)	$V_t = \frac{kT}{e} = 0.0259$ volt $kT = 0.0259$ eV

Table B.6 | Properties of SiO_2 and Si_3N_4 ($T = 300$ K)

Property	**SiO_2**	**Si_3N_4**
Crystal structure	[Amorphous for most integrated circuit applications]	
Atomic or molecular density (cm^{-3})	2.2×10^{22}	1.48×10^{22}
Density ($g\text{-}cm^{-3}$)	2.2	3.4
Energy gap	≈9 eV	4.7 eV
Dielectric constant	3.9	7.5
Melting point (°C)	≈1700	≈1900

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系所：電子系、光電所
科目：電磁學

1. Given a vector function $\mathbf{F}=\mathbf{a}_x(x+c_1z)+\mathbf{a}_y(c_2x-3z)+\mathbf{a}_z(x+c_3y+c_4z)$. Determine the constants c_1, c_2, c_3, and c_4, if F is irrotational and also solenoidal. (15%)

2. The two parallel conducting wires of a power transmission line have a radius a and are spaced at a distance d apart. The wires are at a height h above the ground. Assuming the ground to be perfectly conducting and both d and h to be much larger than a, find the expression for the mutual and self-partial capacitances per unit length. (15%)

3. Consider a plane boundary ($y=0$) between air (region 1, $\mu_{r1}=1$) and iron (region 2, $\mu_{r2}=5000$). Assuming $\mathbf{B}_1=\mathbf{a}_x0.5-\mathbf{a}_y10$ (mT), find $\mathbf{B}_2$ and the angle that $\mathbf{B}_2$ makes with the interface. (20%)

4. The maximum electric field at a distance of 10 m from an isotropic point light source is 2.0 V/m. What are (a) the maximum value of the magnetic field and (b) the average intensity of the light there? (c) What is the power of the source? (15%)

5. A plane electromagnetic wave, with wavelength 3.0 m, travels in vacuum in the positive direction *of an x* axis. The electric field, of amplitude 300 V/m, oscillates parallel to the y axis. What are the (a) frequency? (b) angular frequency, and (c) angular wave number of the wave? (d) What is the amplitude of the magnetic field component? (e) What is the time averaged rate of energy flow in watts per square meter associated with this wave? The wave uniformly illuminates a surface of area 2.0 m^2. (25%)

6. The induced magnetic field 6.0 mm from the central axis of a circular parallel-plate capacitor and between the plates is 2.0×10^{-7} T. The plates have radius 3.0 mm. At what rate $d\vec{E}/dt$ is the electric field between the plates changing? (10%)

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系所：資工所、電子系
科目：計算機概論

1. (5 points) Use the following BNF grammer
<assignment statement> ::= <var> := <expr>
<expr> ::= <var> | <expr> <operation> <var>
<var> ::= X | Y
<operation> ::= + | -
to draw the parse three for the assignment: X:=X+X-Y

2. (10 points) Write a Turing machine and draw the corresponding state diagram that converts all the bits of a binary string from 0 to 1 and 1 to 0, but does not convert the last bit in a string, and stops when it hits the first blank. For example, **b0100100b** is converted to **b1011010b** and **b01101b** is converted to **b10011b.**

3. (10 pints)(a) Explain what a multiplexor circuit does. Be sure to state how many input and output lines it has.
(b) If 11011111 is the input to a multiplexor, give the selector input that would give 0 as an output. (Assume that the input bits are numbered from right to left)

4. (15 points) A typical floppy disk on a PC has the following characteristics:
Rotation speed=3600 rev/min, arm movement time=1 ms fixed startup time +0.1 ms for each track crossed (The 1 ms time is a constant no matter how far the arm moves.) Number of surfaces=2 (a double-sides floppy disk. A single read/write arm holds both read/write heads) Number of tracks per surface=100, Number of sectors per track=20, Number of characters per sector=512
(a)Name and define the three components of access time to any individual sector on a hard disk.
(b)How many characters can be stored on a single floppy disk?
(c)What are the best-case, the worst-case, and the average-case (assume that on the average, the read/write head must move about 30 tracks) access times to any individual sector of this disk?

5. (10 points) What are the outputs of the following C programs?

(a)
```
#include < stdio.h >
#define f(x)(x*x+2*x+9)
void main()
{
    int i=2;
    printf("%d, %d \n", f(i), f(i+1));
}
```

(b)
```
#include < stdio.h >
void main (void)
{
    int i=2, s=0, *pi, *pj;
    int a[12]={4,5,6,1,2,3,7,8,9,7,8,9};
    pi=a;
    pj=pi+1;
    for (i=2 ; i<9; i+=2);
        s+=*(pj+i);
    printf("%d   %d   s=%d\n", *pi, *pj, s);
}
```

(c)
```
#include < stdio.h >
void p1(int *i, int *j)
    {
   *i=*j+5;
   *j=*j-1;
   printf("%d %d \n", *i, *j);
}
void p2(int *a, int b)
    {
   *a+=5;
   b*=2;
   printf("%d %d \n", *a, b);
   p1(a, &b);
}
main( )
    {
   int x=5, y=8;
   p2(&x, y);
   printf("%d %d \n", x,y);
}
```

(d)
```
#include < stdio.h >
main( )
{
   int i, j,cnt=0;
   for( i=1; i<=10; i++) {
        for( j=1; j<=10; j++) {
             if ( i==5) continue;
             if (j>5) break;
             cnt++;
        }
   }
   printf("%d\n",cnt);
}
```

(e)
```
#include <stdio.h>
main ( )
{
   int a=1, b=2, c=3;
   a+=b+=c+=7;
   printf("a=%d, b=%d, c=%d \n",a,b,c);
}
```

6. (10 points) Show the printouts after executing the following C++ statements.

(a)
```
char quiz = 'E';
char * pq = &quiz;
std::cout << *pq;
*pq = 'Q';
std::cout << quiz << std::endl;
```

(b)
```
std::string name = "Gery";
int   i = name.size();
name += "Smith";
std::cout << name[i] << std::endl;
```

7. (10 points) Describe the idea of stored program concept.

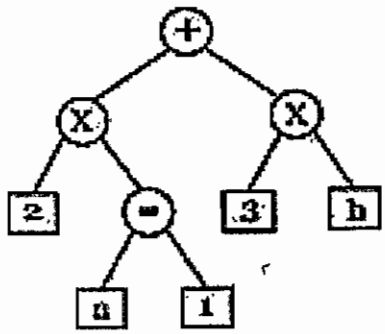
8. (10 points) Determine the total time it would take to transmit a complete gray-scale image (with 8bits/pixel) from a screen with a resolution of 1,000x1,000 pixels using the following media: (a) A V.90 modem (b) A dedicated T1 phone line (c) A dedicated T3 phone line (d) A fiber-optic OC-3 line (e) An OC-48 gigabit line.

9. (10 points) Develop an algorithm that, when given an arrangement of the digits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, will rearrange the digits so that the new arrangement represents the next larger value that can be represented by these digits--otherwise reports that no such rearrangement exists if no rearrangement produces a larger value. Thus, 4317859602 would produce 4317859620.

國立雲林科技大學
94 學年度碩士班入學招生考試試題

系所：資工所、電子系
科目：計算機概論

10. (10 pints) Write a pseudo code to printout an arithmetic expression that is stored in an arithmetic expression tree. The diagram below shows an example of the arithmetic expression tree with the arithmetic expression (2 x (a -1) + (3 x b)).



國立雲林科技大學
94學年度碩士班入學招生考試試題

系所：資工所、電子系
科目：線性代數

1. (10%) Find A^{120} where A is given by

$$A=\begin{bmatrix}1 & 1\\ 1 & 0\end{bmatrix}$$

2. (15%) Find the minimum value of

$$C(x_1,x_2)=\frac{x_1^2-x_1x_2+x_2^2}{2x_1^2+x_2^2}$$

where x_1 and x_2 are both real numbers.

3. (10%) Prove the following statement: If A and B are diagonalizable, they share the same eigenvector matrix S if and only if $AB=BA$.

4. (15%) Find the singular value decomposition of

$$A=\begin{bmatrix}2 & 2\\ -1 & 1\end{bmatrix}$$

5. (15%) Show that the set R^+ of positive reals is a linear space when '$x+y$' is interpreted to mean the product of x and y (so that 2+3 is 6), and '$r\cdot x$' is interpreted as the r-th power of x.

6. (20%) For each of (a), (b) and (c), you must justify your answer with a proof or counter examples:
(a) If A, B are subspaces of a vector space, must $A\cap B$ be a subspace? Always? Sometimes? Never?
(b) Must $A\cup B$ be a subspace?
(c) If A is a subspace, must its complement be a subspace?

7. (15%) Consider the vectors $\vec{v},\vec{s}_1,\vec{s}_2,..\vec{s}_m$ in R^n. Prove
span$(\vec{s}_1,\vec{s}_2,..\vec{s}_m)$=span$(\vec{v},\vec{s}_1,\vec{s}_2,...\vec{s}_m)$ if and only if $\vec{v}\in$ span$(\vec{v},\vec{s}_1,\vec{s}_2,..\vec{s}_m)$.