國立雲林科技大學
九十三學年度碩士班入學招生考試試題

系所：電子系
科目：電子電路

計算題共六題

1. (10%) (1) (5%) What is the highest frequency of a triangle wave of 20-V peak-to-peak amplitude that can be reproduced by an op amp whose slew rate is 10 $V/\mu s$?

   (2) (5%) For a sine wave of the same frequency, what is the maximum amplitude of output signal that remains undistorted?

2. (20%)In the circuit shown in Fig.p2, the transistor has β =100, V_A=200V, and it uses I=1mA and R_B=10MΩ. For this transistor, assume $r_\mu = \beta r_o$.

   (1) (10%)What is the value of r_o?

   (2) (5%)What is the value of r_μ?

   (3) (5%)Estimate the dc voltage at node C.

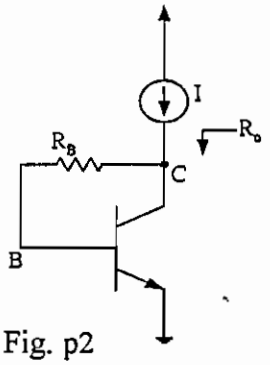

Fig. p2

3. (20%) (1) (10%) If the *pnp* transistor in the circuit of Fig.p3 is characterized by its exponential relationship with a scale current I_S, show that the dc current I is determined by $IR = V_T \ln(I/I_S)$.

   (2) (10%) Assume Q_1 and Q_2 to be matched and Q_3, Q_4, and Q_5 to be matched. Find the value of R that yields a current I =10 μA. For the BJT, V_{EB}=0.7V at I_E=1mA.

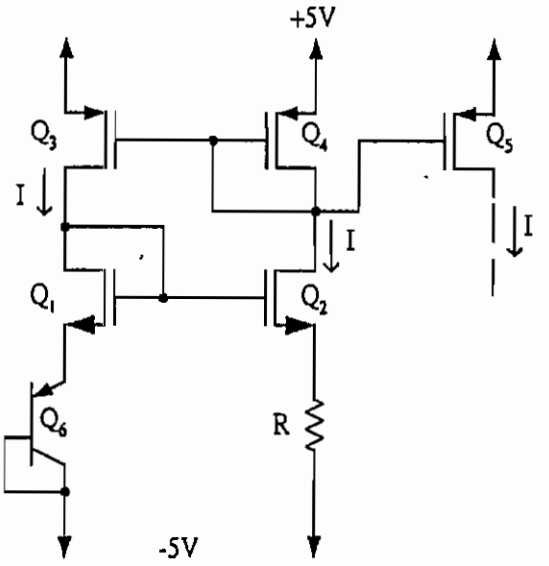

Fig. p3

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系所：電子系
科目：電子電路

4. (20%) For the circuit shown in Fig. P4, V_{os} is the input-referred offset voltage of A_1. Write down $\frac{V_{out}}{V_{os}} = ?$

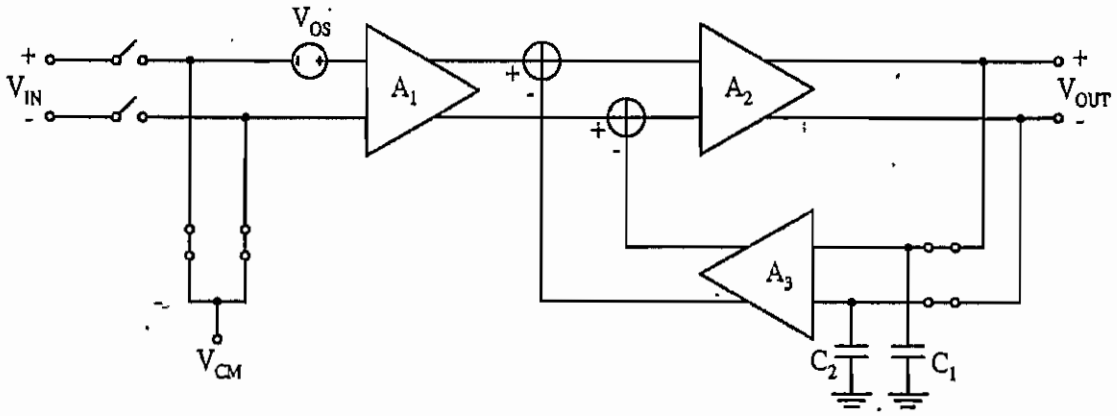

Fig. P4

5. (20%) Neglect the channel-length modulation effect. What is the low-frequency voltage-gain of the amplifier shown in Fig. P5?

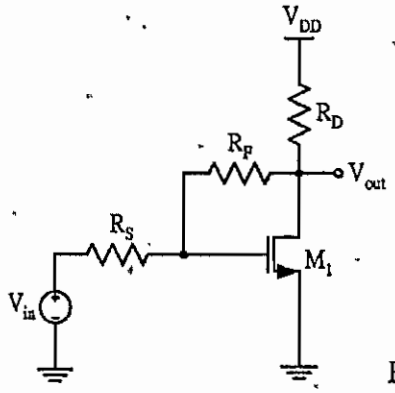

Fig. P5.

6. (10%) Calculate the maximum power conversion efficiency of the circuit shown in Fig. P6. Show your calculation.

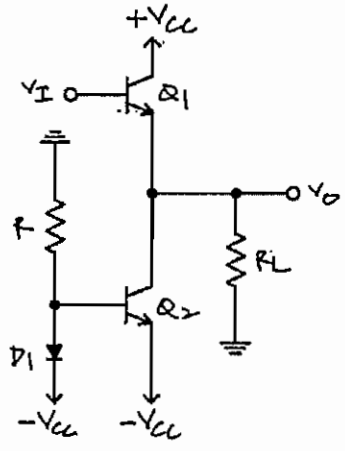

Fig. P6

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系所：電子系
科目：微電子學

總分 100 分

1. Draw the small-signal model of a *pn* diode for both forward and reverse bias and explain the physical meaning of each element in the model. **(15%)**

2. **(a)** Draw the circuit diagrams of the common-base, the common-emitter, and the common collector configurations, respectively, for an *npn* bipolar junction transistor.
   (b) Describe the bias conditions for an *npn* bipolar junction transistor to operate in the active, the cutoff, and the saturation regions, respectively. **(20%)**

3. Make a comparison between the performance of PMOS and NMOS field-effect transistors. **(15%)**

4. For the BJT differential-pair configuration, find the differential signal ($v_d = v_{B1} - v_{B2}$) sufficient to cause
   (a) $i_{C2} = 99\% I$; (b) $i_{C1} = 9.0\, i_{C2}$ **(10%)**

5. Consider a differential amplifier biased with a current source $I = 1$ mA and having $R_C = 10$ kΩ. Let the amplifier be fed with a source having $R_S = 10$ kΩ. Also let the transistors be specified to have $\beta_0 = 100$, $C_\pi = 6$ pF, $C_\mu = 2$ pF, and $r_x = 50$ Ω. Find the dc differential gain A_0, the 3-dB frequency f_H, and the gain bandwidth product. **(30%)**

6. State why negative feedback is applied in amplifier design. **(10%)**

國立雲林科技大學
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系所：電子系
科目：積體電路設計

1. (10 pts) Please explain the following terms briefly
   a) System on a Chip (SoC) (2 pts)
   b) Cell-Based Design (2 pts)
   c) Full Custom Design (2 pts)
   d) Soft Intellectual Property (Soft IP) (2 pts)
   e) Crosstalk (2 pts)

2. (20pts) For the following three CMOS inverter designs
   A: PMOS $(W/L)_p$=1, $(W/L)_n$=2
   B: PMOS $(W/L)_p$=1, $(W/L)_n$=1
   C: PMOS $(W/L)_p$=2, $(W/L)_n$=1
   Assume the transistors have the following parameters

   $$k_p' = 27\mu A/V^2, k_n' = 70\mu A/V^2, V_{TN} = |V_{TP}| = 0.7V, V_{DD} = 5V$$

   a) Please draw the transfer curve of an inverter and define its noise margin high NM_H and noise margin low NM_L (5 pts)
   b) For B inverter, please calculate its noise margin high NM_H (6 pts)
   c) Which of these three inverter designs has the best NM_H? (please justify your answer) (3 pts)
   d) Which of these three inverter designs has the best output rise time delay? (please justify your answer) (3 pts)
   e) Which of these three inverter designs is most suitable to serve as a TTL to CMOS logic buffer? (please justify your answer) (3 pts)

3. (16pts) For the Boolean equation $y = \overline{a \cdot b + c}$
   a) Please draw its circuit schematic using static CMOS full logic (4 pts)
   b) Please draw its circuit schematic using Domino N type logic (4 pts)
   c) For the circuit schematic in a), please draw its Euler graph and identify a common Euler path between N and P blocks (4 pts)
   d) For the Euler path derived in c), assume 1P1M N-well process, please draw its layout (4 pts)

4. (14pts) For the dynamic circuits shown in Figure 1
   a) Please identify the operations of circuit (b) & (c) in each phase and fill in Table 1 with pre-charge (PC), evaluation (EV), or output hold/latched (HD) (8 pts)
   b) Please identify which of the following logic cascades can work properly? (6 pts)
   i) (b) → (a)
   ii) (b) → (c)
   iii) (a) → (c)

Table 1

	ϕ1	ϕ2	ϕ3	ϕ4
(b)				
(c)				

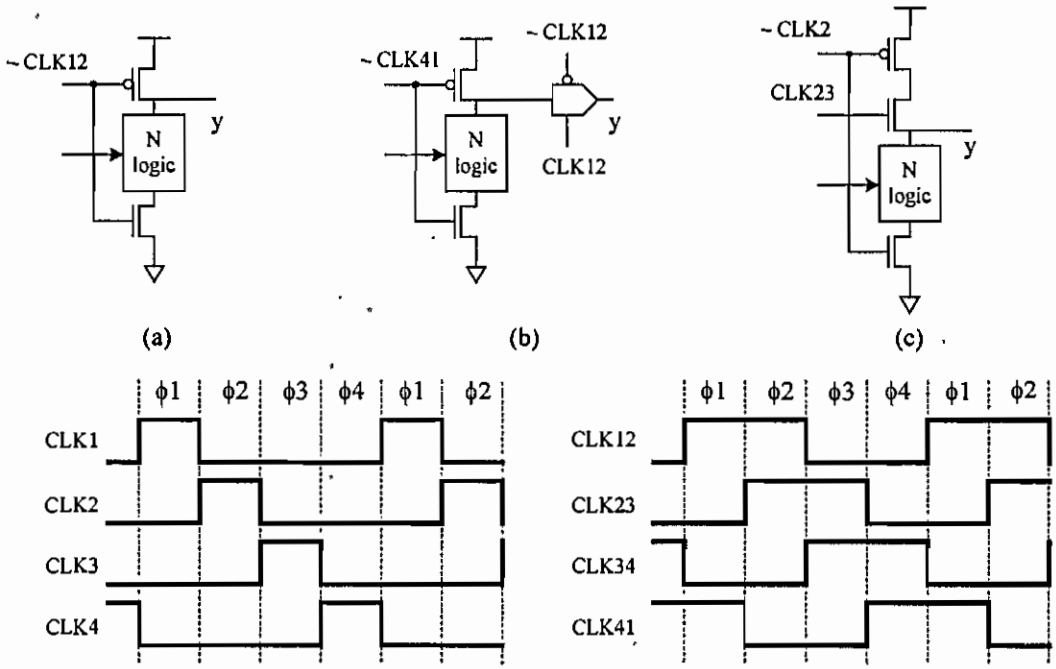

Figure 1

5. (25 pts) Figure 2 shows the inputs and outputs of a 1-bit full adder
   a) Please list its truth table of the 1-bit full adder in Figure 2 (5 pts)
   b) Please draw its circuit schematic using no more than 5 logic gates, where each

gate has two inputs and can be of type AND, OR, or XOR (5 pts)

c) Please write its hardware description language using Verilog® or VHDL language (5 pts)

d) Please write its test file shown in Figure 3 using the Verilog® or VHDL language (5 pts)

e) Please write the 4-bit adder HDL shown in Figure 4 using the module in c) (5 pts)

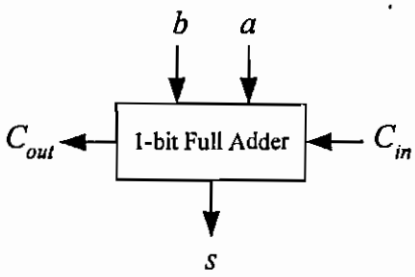

Figure 2

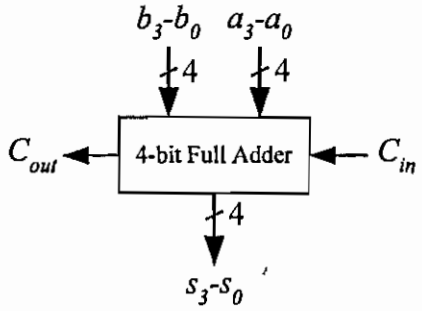

Figure 4

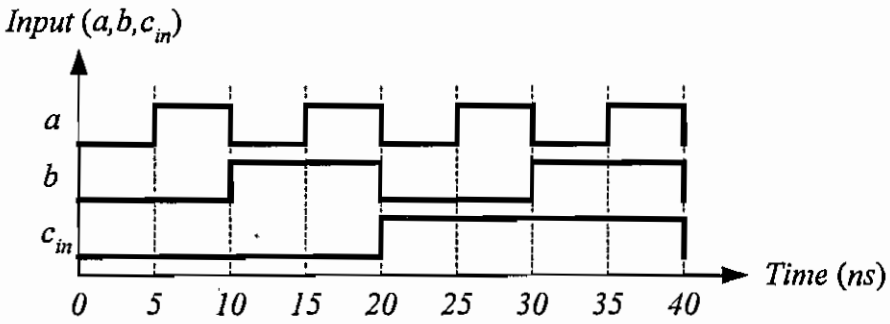

Figure 3

6. (15 pts) Please draw the following circuit schematics

a) Positive Latch (5 pts)

b) Multiplexer-based NMOS Latch (5pts)

c) Master-slave positive edge-trigger register (5 pts)

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系所：電子系
科目：線性代數

1. (15%) Find the least-squares solution $\vec{x}^*$ of the system

$$\mathbf{A}\vec{x} = \vec{b}, \text{ where } \mathbf{A} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \end{bmatrix} \text{ and } \vec{b} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}.$$

and draw a sketch showing the vector $\vec{b}$, the image of $\mathbf{A}$, the vector $\mathbf{A}\vec{x}^*$, and the vector $\vec{b} - \mathbf{A}\vec{x}^*$.

2. Let V be the linear space of all functions of the form $f(x) = a\cos(x) + b\sin(x)$, which is a subspace of C^∞. Consider the linear transform

$$T(f) = f'' + 2f' - 3f$$

from V to V.

(a) (5%) Find the matrix $\mathbf{B}$ of T with the respect to the basis $\mathcal{B}$ consisting of functions $\cos(x)$ and $\sin(x)$.

(b) (10%) Please solve the differential equation $f''(x) + 2f'(x) - 3f(x) = \cos(x)$.

3. In a digital system, addition and multiplication are defined as usual, except for rule $1+1=0$. We denote this number system with $\mathbf{F}$. The set of all vectors with n components in $\mathbf{F}$ is denoted by $\mathbf{F}^n$. A Hamming matrix with m rows is a matrix that contains all nonzero vectors in $\mathbf{F}^m$ as its columns in any order. Here is an example:

$$\mathbf{H} = \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 1 & 1 & 0 \end{bmatrix},$$

(a) (5 %) Express the kernel of $\mathbf{H}$ as the span of four vectors in $\mathbf{F}^7$ of the form $\vec{v}_1$, $\vec{v}_2$, $\vec{v}_3$, and $\vec{v}_4$, where

$$\vec{v}_1^T = [* \ * \ * \ 1 \ 0 \ 0 \ 0], \ \vec{v}_2^T = [* \ * \ * \ 0 \ 1 \ 0 \ 0],$$

$$\vec{v}_3^T = [* \ * \ * \ 0 \ 0 \ 1 \ 0], \ \vec{v}_4^T = [* \ * \ * \ 0 \ 0 \ 0 \ 1].$$

(b) (5 %) There is another 7×4 matrix

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系所：電子系
科目：線性代數

$$\mathbf{M}=\begin{bmatrix} | & | & | & | \\ \vec{v}_1 & \vec{v}_2 & \vec{v}_3 & \vec{v}_4 \\ | & | & | & | \end{bmatrix},$$

If $\vec{x}$ is an arbitrary vector in $\mathbf{F}^4$, what is $\mathbf{HM}\vec{x}$?

(c) (10 %) A vector $\vec{u}$ in $\mathbf{F}^4$ is first transformed into a vector $\vec{v}=\mathbf{M}\vec{u}$ in $\mathbf{F}^7$, where $\mathbf{M}$ is the matrix used in (b). The vector $\vec{v}$ is now transmitted over a channel. We assume that at most one error will occur during transmission; that is, the received vector $\vec{w}$ will be either $\vec{v}$ or $\vec{w}=\vec{v}+\vec{e}_i$, where $\vec{e}_i$ denotes an error in the ith bit of the vector. Suppose the vector $\vec{w}^T=\begin{bmatrix}1 & 0 & 1 & 0 & 1 & 0 & 0\end{bmatrix}$ is received. Determine whether an error was made in the transmission and if so, correct it.

4. (20%) Find the eigenvalues of the matrix A given by

$$A=\begin{bmatrix} 5 & 3\cos(\frac{7\pi}{6}) & 3\cos(\frac{14\pi}{6}) & 3\cos(\frac{21\pi}{6}) & 3\cos(\frac{28\pi}{6}) & 3\cos(\frac{35\pi}{6}) \\ 3\cos(\frac{7\pi}{6}) & 5 & 3\cos(\frac{7\pi}{6}) & 3\cos(\frac{14\pi}{6}) & 3\cos(\frac{21\pi}{6}) & 3\cos(\frac{28\pi}{6}) \\ 3\cos(\frac{14\pi}{6}) & 3\cos(\frac{7\pi}{6}) & 5 & 3\cos(\frac{7\pi}{6}) & 3\cos(\frac{14\pi}{6}) & 3\cos(\frac{21\pi}{6}) \\ 3\cos(\frac{21\pi}{6}) & 3\cos(\frac{14\pi}{6}) & 3\cos(\frac{7\pi}{6}) & 5 & 3\cos(\frac{7\pi}{6}) & 3\cos(\frac{14\pi}{6}) \\ 3\cos(\frac{28\pi}{6}) & 3\cos(\frac{21\pi}{6}) & 3\cos(\frac{14\pi}{6}) & 3\cos(\frac{7\pi}{6}) & 5 & 3\cos(\frac{7\pi}{6}) \\ 3\cos(\frac{35\pi}{6}) & 3\cos(\frac{28\pi}{6}) & 3\cos(\frac{21\pi}{6}) & 3\cos(\frac{14\pi}{6}) & 3\cos(\frac{7\pi}{6}) & 5 \end{bmatrix}$$

5. (20%) Find a matrix B that simultaneously diagonalize

$$P=\begin{bmatrix}2 & 1\\ 1 & 2\end{bmatrix} \quad \text{and} \quad Q=\begin{bmatrix}3 & -1\\ -1 & 3\end{bmatrix}$$

6. (10%) Prove that the maximum value of $\underline{x}^T A\underline{x}$ equals the maximum eigenvalue of A, where A is an $N\times N$ real symmetric matrix and $\underline{x}$ is any nonzero $N\times 1$ real vector with a unity norm, i.e., $\underline{x}^T\underline{x}=1$

國立雲林科技大學
九十三學年度碩士班入學招生考試試題

系所：電子系
科目：計算機組織

1. Suppose a program runs on a processor with a base CPI of 1, when all memory accesses hit in the cache, and a clock rate of 500 MHz. If a program has 40% of the instructions are data accesses (loads and stores). Assume a main memory access time of 200 ns, including the miss handling.
   (a) What is the CPI when the cache miss rate is 100% ? (10%)
   (b) What is the CPI when the cache miss rate is 5%? (10%)

2. The performance of a 200 MHz microprocessor P is measured by execution 10,000,000 instructions of benchmark code, which is found to take 0.25 s.
   (a) What is the value of CPI? (5%)
   (b) What is the MIPS of the microprocessor P? (5%)

3. A 32-bit big-endian CPU with 24-bit address line, can generate BHE0#, BHE1#, BHE2#, and BHE3# signals for the section enable signal (the symbol # means active low). Please use 128k*8-bit SRAM (have two active low chip-select input) to construct a 2-way double-word interleaved memory system which is located in 0x800000 ~ 0xBFFFFF address range. (10%)

4. A cache system consists of 8 blocks. Each cache block size is 4-byte and the initial value is empty. Assume the cache system is a two-way set associated with LRU (least recently used) replacement policy. Way 0 is used first for a set. If the CPU generates the following addresses to read a data: 1, 5, 8, 3, 40, 17, 19, 56, 49, 43, what of the address read is hit or miss? (10%)

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系所：電子系
科目：計算機組織

5. Assume that the processor executes with a 500MHz clock. The hard disk transfers data in four-word chunks and can transfer at 4MB/sec. No transfer can be missed. Determine the fraction of CPU time consumed for the polling, Interrupt-driven I/O, and DMA:
   (a) Assume that the number of clock cycles for a polling operation is 400. (4%)
   (b) Assume that we use interrupt-driven I/O, the hard disk overhead for each transfer is 500 clock cycles and it is only transferring data 5% of the time. (4%)
   (c) Assume that the initial setup of a DMA transfer takes 1000 clock cycles for the processor, and the handling of the interrupt at DMA completion requires 500 clock cycles for the processor. IF the average transfer from the disk is 8 KB, what fraction of the 500MHz processor is consumed if the disk is actively transferring 100% of the time? (5%)
6. You are going to enhance a machine, and there are two possible improvements: either makes multiply instructions run four times faster than before, or make memory access instructions run two times faster than before. You repeatedly run a program that takes 100 seconds to execute. Of this time, 20% is used for multiplication, 50% for memory access instructions, and 30% for other tasks. What will the speedup be if you improve only multiplication? What will the speedup be if you improve only memory access? What will the speedup be if both improvements are made? (10%)
7. Please use full adders and exclusive-OR gate to design a 4-bit adder-subtractor circuit. The circuit input M controls the operation. When M=0 the circuit is an adder and when M = 1 the circuit becomes a subtractor. (10%)
8. Consider a memory hierarchy using one of the three organizations for memory shown in Fig. 1. Assume that the cache block size is 16 words, the width of organization b of Fig. 1 is four words, and the number of banks in organization c is four. If the main memory latency for a new access is 10 cycles and the transfer time is 1 cycle.
   (a) What are the miss penalties for each of these organizations? (6%)
   (b)Suppose a processor with a 16-word block size has an effective miss rate per instruction of 0.5%. Assume that the CPI without cache misses is 1.2. How much faster is this processor when using the wide memory than when using narrow or interleaved memories? (6%)

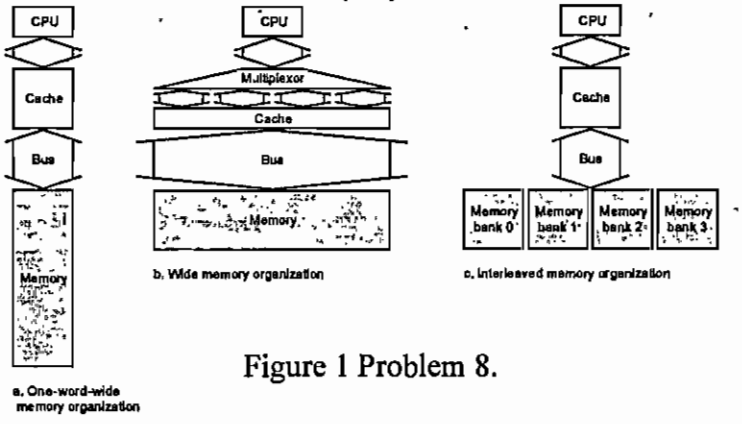

Figure 1 Problem 8.

9. Using zero-address machine to compute $X=(A+B)\times(C+D)+E$. The instructions available for use are as follows: ***PUSH M, POP M, ADD, SUB, MUL, DIV.*** (5%)

國立雲林科技大學
九十三學年度碩士班入學招生考試試題

系所：電子系、光電所
科目：半導體元件

1. A silicon pn junction diode is doped with $N_d = N_a = 10^{18}$ cm^{-3}, Zener breakdown occurs when the peak electric field reaches 10^6 V/cm. Determine the reverse-bias breakdown voltage. (20%)

2. To calculate the theoretical barrier height, built-in potential barrier, and maximum electric field in a metal-semiconductor diode for zero applied bias. Consider a contact between tungsten and n-type silicon doped to $N_d = 10^{16}$ cm^{-3} at $T = 300$ K. (The metal work function for tungsten is 4.55 volts and the electron affinity for silicon is 4.01 volts.). (20%)

3. The following currents are measured in a uniformly doped npn bipolar transistor:

   $I_{nE} = 1.20$ mA $I_{pE} = 0.01$ mA $I_{nC} = 1.18$ mA
   $I_R = 0.005$ mA $I_G = 0.001$ mA $I_{pc0} = 0.001$ mA

   Assume that the active cross-sectional area is the same for the collector and emitter.
   (a) Determine the emitter injection efficiency factor γ. (5%)
   (b) Determine the base transport factor α_T. (5%)
   (c) Determine the recombination factor δ. (5%)
   (d) Determine small-signal common emitter current gain β. (5%)

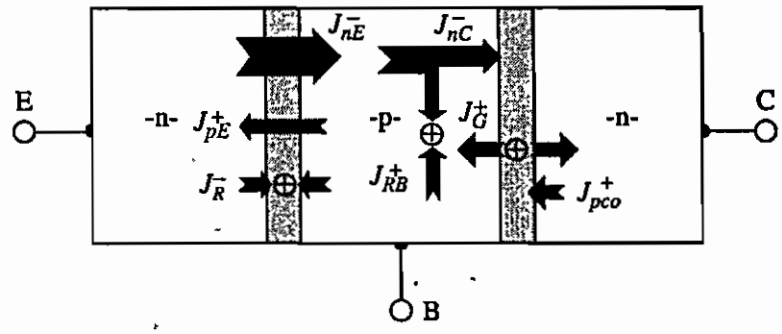

Figure for question 3: Particle current density in an npn bipolar transistor operating in the forward-active mode.

4. Consider an MOS system formed by an n^+ polysilicon gate and a p–type silicon substrate doped to $N_a = 5 \times 10^{16}$ cm^{-3}. Assuming $Q'_{ss} = 10^{11}$ cm^{-3} and the work function difference is –1.12V. Determine the oxide thickness such that $V_{TN} = +0.63$ V. $T = 300$ K. (20%).

5. For an n-channel MOSFET:

(a) What is subthreshold conduction? What is the current-voltage relation of this effect? (7%)

(b) What is short-channel effect? How does the channel length affect the transistor? (7%)

(c) Explain the substrate bias effect. (6%)

Table B.4 | Silicon, gallium arsenide, and germanium properties ($T = 300$ K)

Property	Si	GaAs	Ge
Atoms (cm^{-3})	5.0×10^{22}	4.42×10^{22}	4.42×10^{22}
Atomic weight	28.09	144.63	72.60
Crystal structure	Diamond	Zincblende	Diamond
Density (g/cm^{-3})	2.33	5.32	5.33
Lattice constant (Å)	5.43	5.65	5.65
Melting point (°C)	1415	1238	937
Dielectric constant	11.7	13.1	16.0
Bandgap energy (eV)	1.12	1.42	0.66
Electron affinity, χ (volts)	4.01	4.07	4.13
Effective density of states in conduction band, N_c (cm^{-3})	2.8×10^{19}	4.7×10^{17}	1.04×10^{19}
Effective density of states in valence band, N_v (cm^{-3})	1.04×10^{19}	7.0×10^{18}	6.0×10^{18}
Intrinsic carrier concentration (cm^{-3})	1.5×10^{10}	1.8×10^{6}	2.4×10^{13}
Mobility (cm^2/V-s)			
Electron, μ_n	1350	8500	3900
Hole, μ_p	480	400	1900
Effective mass $\left(\frac{m^*}{m_0}\right)$			
Electrons	$m_l^* = 0.98$	0.067	1.64
	$m_t^* = 0.19$		0.082
Holes	$m_{lh}^* = 0.16$	0.082	0.044
	$m_{hh}^* = 0.49$	0.45	0.28
Effective mass (density of states)			
Electrons $\left(\frac{m_n^*}{m_0}\right)$	1.08	0.067	0.55
Holes $\left(\frac{m_p^*}{m_0}\right)$	0.56	0.48	0.37

Table B.3 | Physical constants

Avogadro's number	$N_A = 6.02 \times 10^{+23}$ atoms per gram molecular weight
Boltzmann's constant	$k = 1.38 \times 10^{-23}$ J/K $= 8.62 \times 10^{-5}$ eV/K
Electronic charge (magnitude)	$e = 1.60 \times 10^{-19}$ C
Free electron rest mass	$m_0 = 9.11 \times 10^{-31}$ kg
Permeability of free space	$\mu_0 = 4\pi \times 10^{-7}$ H/m
Permittivity of free space	$\epsilon_0 = 8.85 \times 10^{-14}$ F/cm $= 8.85 \times 10^{-12}$ F/m
Planck's constant	$h = 6.625 \times 10^{-34}$ J-s $= 4.135 \times 10^{-15}$ eV-s $\frac{h}{2\pi} = \hbar = 1.054 \times 10^{-34}$ J-s
Proton rest mass	$M = 1.67 \times 10^{-27}$ kg
Speed of light in vacuum	$c = 2.998 \times 10^{10}$ cm/s
Thermal voltage ($T = 300$ K)	$V_t = \frac{kT}{e} = 0.0259$ volt $kT = 0.0259$ eV

Table B.6 | Properties of SiO_2 and Si_3N_4 ($T = 300$ K)

Property	SiO_2	Si_3N_4
Crystal structure	[Amorphous for most integrated circuit applications]	
Atomic or molecular density (cm^{-3})	2.2×10^{22}	1.48×10^{22}
Density (g-cm^{-3})	2.2	3.4
Energy gap	≈9 eV	4.7 eV
Dielectric constant	3.9	7.5
Melting point (°C)	≈1700	≈1900

國立雲林科技大學
九十三學年度碩士班入學招生考試試題

系所：電子系
科目：電磁學

本試卷共七大題，總分 100 分。

1. Find the magnetic moment $\vec{m}$ of a circular disc of radius x thickness $\triangle y$, and uniform volume charge density ρ. Assume the disc is spinning with angular velocity ω.(15 分)

2. In a coaxial cable current I flows down the center conductor and back through the outer conductor. Let *V* be the voltage between the conductors. Show that the power flows through the space between the conductors and that its value equals *VI*.(15 分)

3. (a) Derive an approximate expression for the magnetic energy *W* in a toroidal solenoid carrying current *i* in its *N* turns. Assume its toroidal radius x_t is much larger than its core radius x_c and in the core $\mu \gg \mu_0$. (10 分)
   (b) Is this magnetic energy stored outside the toroid, in the core,or in the wire, why ? (5 分)

4. Suppose that E is given by the expression

$$\vec{E} = -\frac{K}{r}\vec{u}_r$$

Where r is the radial distance from the origin and $\vec{u}_r$ is the unit vector pointing out along this radius. Derive an expression for the potential difference *V* between points at distance r_2 and r_1 from the origin. (10 分)

5. Two infinite parallel plates are separated by a distance s. The top one is at potential V_s and the bottom one at potential V_0.
   (a)Write Poisson's equation, how apply it for this case. (5 分)
   (b)Find an expression for the potential *V* between the plates. (5 分)
   (c)Find an expression for the electric field E between the plates. (5 分)

6. By using the Biot-Savart law, derive the magnetic flux density $\vec{B}$ at a point distance on the axis from the center of a circular loop of current.(15 分)

7. Derive the expression for the force $\vec{F}$ on an electric dipole with moment $\vec{p}$ in an electric field $\vec{E}$ in which $E_x = 0$, $p_x = 0$, and p is a constant. (15 分)

國立雲林科技大學
九十三學年度碩士班入學招生考試試題

系所：資工所、電子系
科目：計算機概論

1. (10 points) Give an advantage that
   (a) a sequential file has over an indexed file
   (b) a sequential file has over a hashed file
   (c) a indexed file has over a sequential file
   (d) a indexed file has over a hashed file
   (e) a hashed file has over a sequential
   (f) a hashed file has over a indexed file

2. (10 points) Design an algorithm that lists all possible rearrangements of the symbols in a string of five distinct characters.

3. (10 points) Arrange the names Bi, Di, Ri, Si, Ti, and Wi in an order that requires the least number of comparisons when sorted by the quick sort algorithm.

4. (10 points) Describe what is the stored-program concept.

5. (10 points) Would a large array probably be passed to a subroutine by value? Yes or No? Support your judgment.

6. (10 points) Draw a state diagram and write the Turing instructions for a Turing machine that takes any string of 1s and changes every third 1 to a 0. Thus, for example,
   ...b111111b...
   would become
   ...b110110b...

7. (15 points) Implement the combination logic $F(A,B,C,D)=\Sigma(0,3,8,10,12,14)+d(1,2,5,7)$
   (a)by using 3 level NAND gate (using minimal number of gates)
   (b)by using a decoder
   (c)by using a 8×1 multiplexor.

8. (5 points) Describe the difference between syntax, run-time, and logic errors.

9. (20 points)Given the following list: 14,15,5,9,8,3,19,4
   (a)Please construct a binary search tree for the sequence.
   (b)Please traverse the binary search tree in postorder.
   (c)Construct an AVL tree for the sequence.
   (d)Construct a heap tree (note, the root has the maximum key) for the sequence.
   (Note. Show your answers step by step.)

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系所：資工所、電子系
科目：作業系統

請依題號作答並將答案寫在答案卷上，違者不予計分。

題目1至題目10爲多選題，每題5分。每題已暗示有幾個答案，但需全部答對才給分，答錯倒扣1分。

1. Which are privileged instructions? (2個答案)
   (A) I/O instruction
   (B) trap or software-generated interrupt
   (C) WAIT instruction
   (D) the base and limit registers (for memory space) loading

2. Which are correct for real-time systems? (3個答案)
   (A) In hard real-time systems, the operating system kernel delays do not need to be bounded.
   (B) A hard real-time system guarantees that critical tasks be completed on time.
   (C) Virtual memory is almost never found on hard real-time systems.
   (D) A soft real-time system claims that a critical real-time task gets priority over other tasks, and retains that priority until it completes.

3. Which activities should be taken in the secondary-storage management? (2個答案)
   (A) free-space management
   (B) creating and deleting directories
   (C) storage allocation
   (D) buffering

4. Which are correct for process states? (2個答案)
   (A) If a process is created, it will enter the "running" state.
   (B) If the waiting event of a process occurs, the process will enter the "running" state.
   (C) If a running process executes I/O, it will enter the "waiting" state.
   (D) If a running process encounters an interrupt, it will enter the "ready" state.

5. Which are correct for CPU-scheduling algorithms? (3個答案)
   (A) The FCFS scheduling algorithm must be nonpreemptive.
   (B) The SJF algorithm must be preemptive.
   (C) An SJF algorithm is simply a priority algorithm where the priority is the inverse of the next CPU burst.
   (D) The round-robin scheduling algorithm is designed especially for time-sharing systems.

6. Which are correct for process synchronizations? (3個答案)
   (A) A semaphore, apart from initialization, is accessed only through two standard atomic operations: wait and signal.
   (B) Mutual-exclusion can be implemented with TestAndSet or Swap instructions.
   (C) A spinlock (some kind of semaphores) is not useful when locks are expected to be held for short time.
   (D) A counting semaphore can be implemented using binary semaphores.

7. What conditions does the approach (i.e., imposing a total ordering of all resource types, and requiring that each process requests resources in an increasing order of enumeration) try to prevent? (1個答案)
   (A) mutual exclusion
   (B) circular wait
   (C) no preemption
   (D) hold and wait

8. Which are correct for pure segmentation? (3個答案)
   (A) Segmentation is a memory-management scheme that supports the user view of memory.
   (B) A particular advantage of segmentation is the association of protection with the segment.
   (C) An advantage of segmentation involves the sharing of code or data.
   (D) Like paging, segmentation has no external fragmentation.

9. Which are correct for virtual memory? (2個答案)
   (A) FIFO page replacement is a stack algorithm.
   (B) The LRU strategy is the optimal page-replacement algorithm looking backward in time, rather than forward.
   (C) The accuracy of the working set depends on the selection of Δ (i.e., the working-set window).
   (D) If I/O is done to or from user virtual memory, these pages do not need to be locked in memory when demand paging is used.

10. Which disk scheduling algorithms always service I/O requests in only one direction? (1 個答案)
   (A) SSTF scheduling
   (B) SCAN scheduling
   (C) C-SCAN scheduling
   (D) LOOK scheduling

11. The following code is designed to solve the Dining Philosopher Problem. Suppose that there are five philosophers spending their lives alternatively thinking and eating spaghetti, and they are seated around a table on which is placed five plates of pasta and five forks. When a philosopher decides to eat, then he or she must obtain two forks by first picking up the left fork and then picking up the right fork. After consuming food, the philosopher replaces the forks and resumes thinking. What problems would occur in the following code executed by each philosopher? Modify the code to solve the problems posed by you. (20%)

```
Semaphore fork [5] = {1, 1, 1, 1, 1};

Philosopher (int i) {
 While (True) {
    ... /* Thinking */
      P(fork[i]);              /* pick up left fork */
      P(fork[(i+1) mod 5]; /* pick up right fork */
       eat( );
      V(fork[(i+1) mod 5];
      V(fork[i]);
 }
```

12. Consider the following page reference string:
    1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6
    How many page faults would occur for the following replacement algorithms: LRU replacement, FIFO replacement, Optimal replacement. Assuming the number of allocated frames is three and all frames are initially empty. (15%)

13. Consider the problem of jobs waiting in a queue until sufficient memory becomes available for them to be loaded and executed. If the queue is a simple first-in-first-out structure, then only the job at the head of the queue may be considered for placement in storage. On the other hand, with a more complex queuing mechanism, it might be possible to examine the entire queue to choose a job to be loaded and executed. Show how the latter discipline, even though more complex, might yield better throughput than the simple first-in-first-out strategy. (15%)