



計算題共六題

- (10%) A current amplifier for which  $R_i = 1\text{k}\Omega$ ,  $R_o = 10\text{k}\Omega$ , and  $A_{is} = 100\text{A/A}$  is to be connected between a 100-mV source having a resistance of  $100\text{k}\Omega$  and a load of  $1\text{k}\Omega$ . What are the values of current gain  $i_o/i_i$ , of voltage gain  $v_o/v_s$ , and of power gain, expressed directly and in dB?
- (20%) Consider the source-follower circuit and its small-signal equivalent circuit of Fig.p2 when fabricated in a technology with  $k'_n = 20\ \mu\text{A/V}^2$ ,  $V_t = 1\text{V}$ , and  $V_A = 100\text{V}$ . Let  $W/L = 10$  for all transistors,  $I_{REF} = 200\ \mu\text{A}$ , and  $\chi = 0.1$ .
  - Find  $g_{m1}$ ,  $r_{o1}$ ,  $r_{o2}$ ,  $A_v$ , and  $R_o$ . (10%)
  - What will the voltage gain become if the output is connected to a 10-k $\Omega$  resistance? (10%)

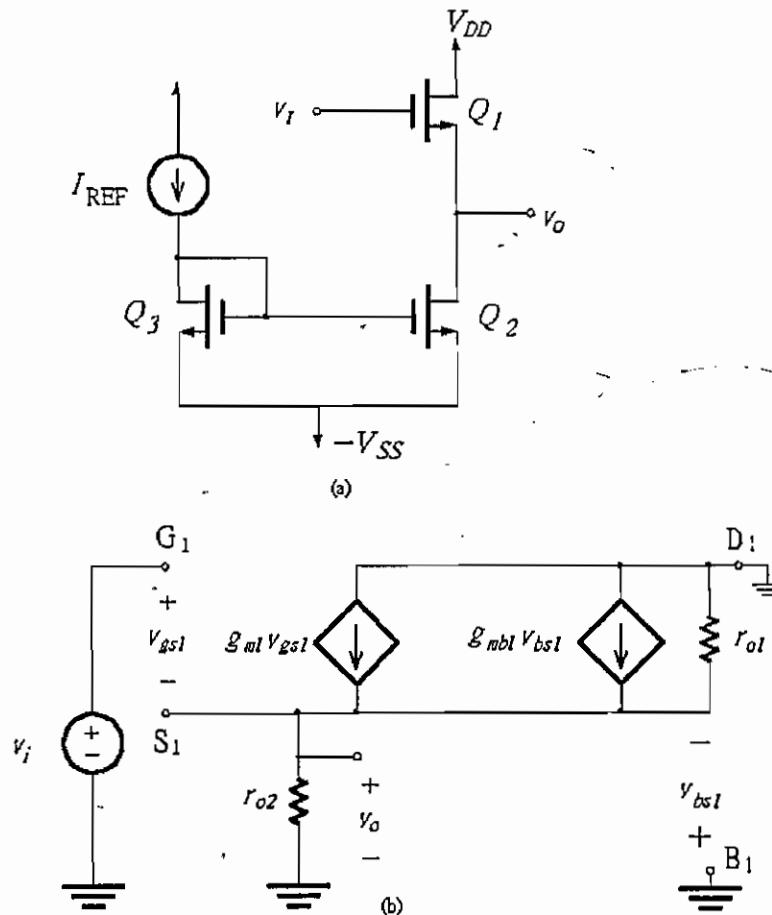


Fig. p2

- (20%) The amplifier in Fig.p3 is biased to operate at  $I_D = 1\text{mA}$  and  $g_m = 1\text{mA/V}$ . Neglecting  $r_o$ ,
  - Find the midband gain. (4%)
  - Find the value of  $C_s$  that place the corresponding pole at 10Hz. (4%)
  - What is the frequency of the transfer-function zero introduced by  $C_s$ ? (4%)



- d. Give an expression for the gain function  $V_o(s)/V_i(s)$ . (4%)
- e. What is the gain of the amplifier at dc? (4%)

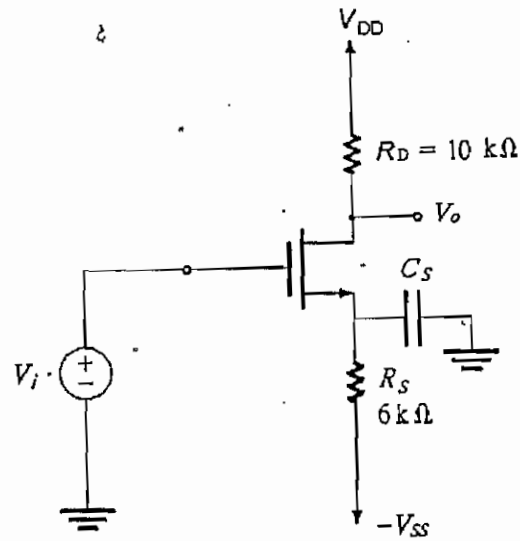


Fig. p3



4. (20%) An electronic circuit is shown in Fig. P4. The amplifier is an ideal voltage amplifier with a DC gain of  $-A$ , where  $A \gg 1$ . Please find the low-frequency closed-loop gain.

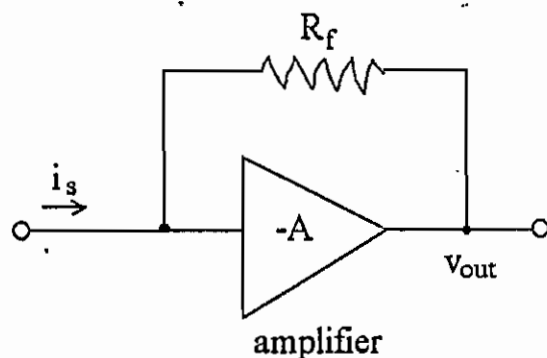


Fig. P4

5. (20%) For the electronic circuit shown in Fig. P5, please find the input impedance. You may neglect the channel-length modulation effect of the MOS transistors. Ignore the parasitic capacitances of the MOS transistors.

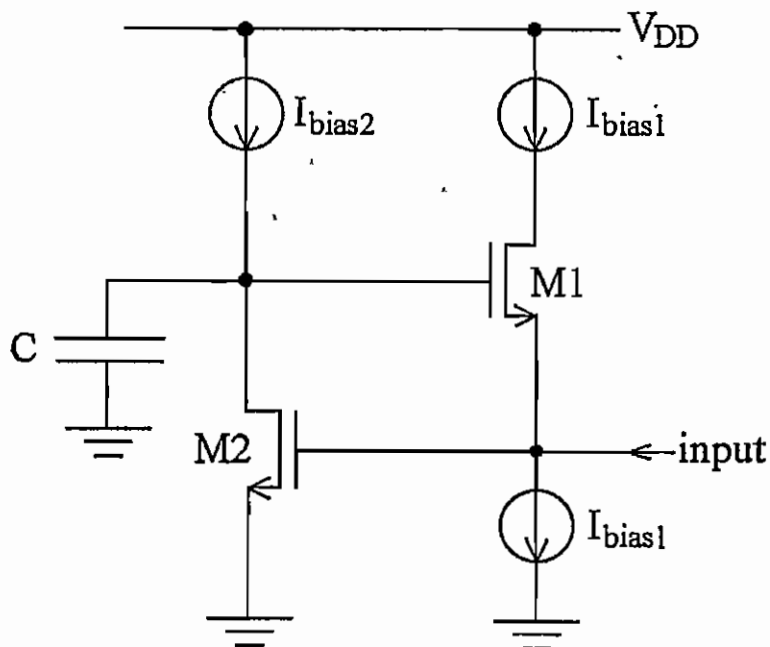


Fig. P5



6. (10%) For the amplifier shown in Fig. P6, please sketch the magnitude of the voltage gain as a function of frequency. The MOS transistor is assumed biased in the saturation region. You may neglect the channel-length modulation effect of the MOS transistor. The transconductance of the MOS transistor is  $10^{-2}$  A/V.

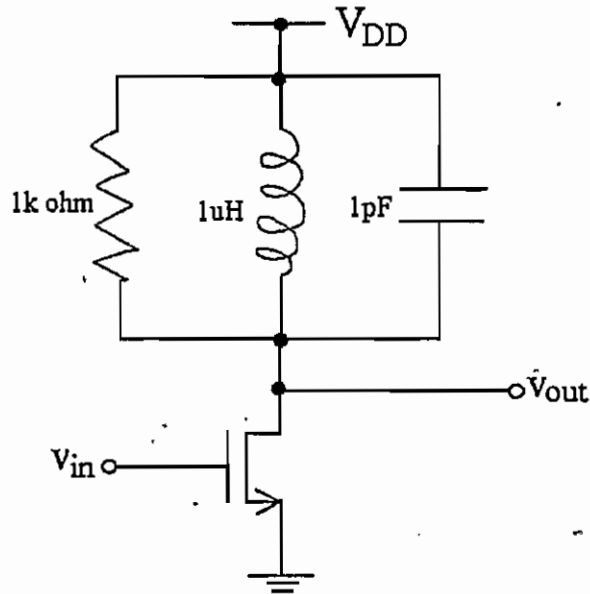


Fig. P6



1. (16pts) Please explain the following terms briefly.

- a) charge sharing
- b) latch up
- c) ratioed logic
- d) body effect
- e) guard ring
- f) abutting substrate contact
- g) minimum spacing of n+ to p+ gate (explain the meaning of this design rule)
- h) LVS

2. (12pts) For the MOS logic listed in Table 1, please check the appropriate table entries with “✓” if the statement regarding the logic is correct

	Pseudo NMOS	Domino logic	CVSL	Zipper logic	Clocked CMOS
Ratioed logic					
Charge sharing problem					
Static power consumption					
Output latch					
Reduced output voltage swing					
Clock input					
Dual rail logic					

Table 1.

3. (12pts) For the circuit shown in Figure 1

- a) please derive its Boolean logic
- b) please draw its stick diagram for the N Logic using a single strip of diffusion
- c) please convert the circuit to its P-type domino circuit counterpart

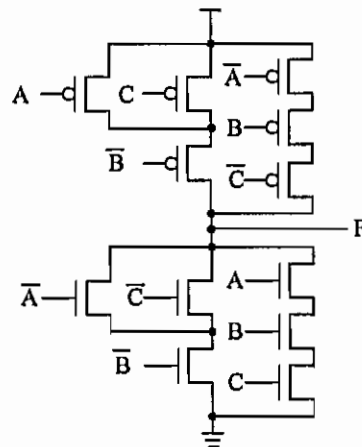


Figure 1.



4. (10pts) For a CMOS inverter with  $\beta_n = 2.4mA/V^2$  and  $\beta_p = 1.8mA/V^2$ . The threshold voltages are given as  $V_{Tn} = 0.6V$ ,  $V_{Tp} = -0.7V$  and the power supply is  $V_{DD} = 3.3V$ . Assume the output node parasitic capacitance is 60fF
- please find the midpoint voltage (or inversion voltage)  $V_M$  ( $V_{inv}$ )
  - please calculate the rise time and the fall time of the design
5. (14pts) For the circuit shown in Fig. 2, the circuit is part of a video processing system that requires a new sample to be processed every 70 nsec. Table 2 enumerates area and the capacitance switched per operation. The multiplier has a delay of 30 nsec at 5 V, and the adder has a delay of 15 nsec at 5 V. Assume negligible the delay, area and power dissipation of registers.
- (8pts) What is the total area? What is the total power dissipated by the circuit?
  - (6pts) Suppose that we pipeline the circuit in Fig. 2 into two stages (each stage has one multiplier and one adder) and the supply voltage enable to be reduced to 3.5 V. What is the power consumption of this new circuit?

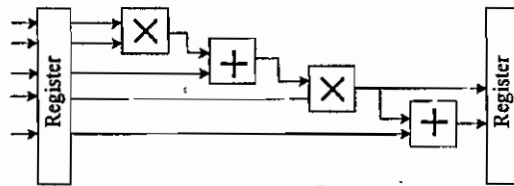


Fig. 2 Arithmetic circuit

Unit	Width*Height (microns)	Capacitance/operation
Multiplier	1600*1500	25 pF
Adder	690*210	1.4 pF

Table 2: Module library

6. (12pts) For the circuit shown in Figure 3,
- (3pts) Does this circuit still function as a tri-state buffer?
  - (6pts) For the  $In$  and  $En$  waveforms given in the figure, sketch the voltages at nodes X, Y, and out. Label asymptotic voltages, neglecting body effect.
  - (3pts) why is this circuit dangerous to use in practice?

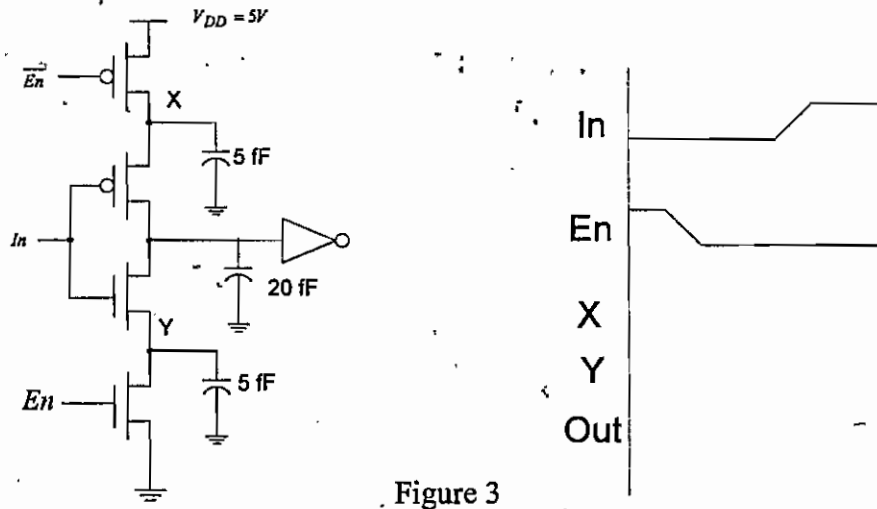


Figure 3

7. (14pts) An adjustable duty-cycle clock generator is shown in Figure 4. Assume the delay through the delay element matches the delay of the multiplexer.
- (8pts) Draw the signal waveform and describe the operation of this circuit
  - (6pts) What range of duty-cycle that can be achieved with this circuit

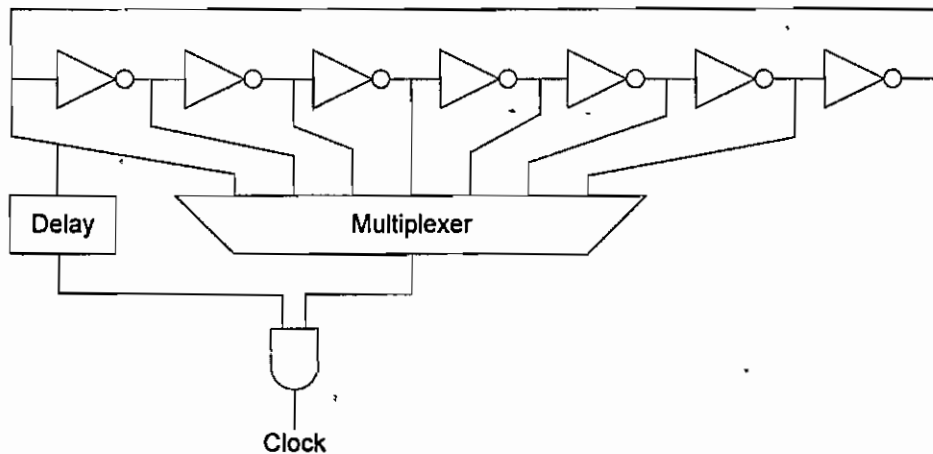


Figure 4. Clock duty-cycle generator



8. (10pts) A two-transistor memory cell is shown in Figure 5. It uses two identical transistors ( $M_1$  and  $M_2$ ) with  $W/L=1.8/1.2$ . Separate lines are provided for the read select (RS) and write select (WS). Please explain the operation of the memory and draw waveform for WB, RB, WS and RS for both reads and writes.

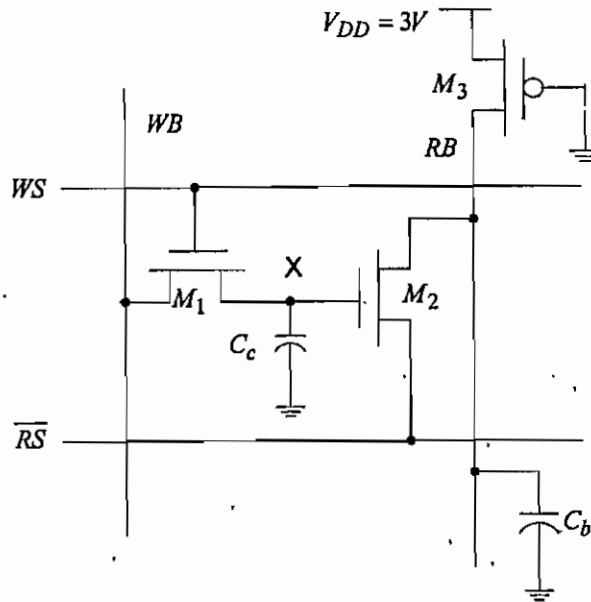


Figure 5. 2-T memory cell





1. The following matrix is a projection matrix:

$$P = \frac{1}{21} \begin{bmatrix} 1 & 2 & -4 \\ 2 & 4 & -8 \\ -4 & -8 & 16 \end{bmatrix}$$

- (a) (5 %) What subspace does  $P$  project onto?  
 (b) (5 %) What is the distance from that subspace to  $(1, 0, 0)$ ?  
 (c) (10 %) Is  $P$  diagonalizable?

2. This equation  $Ax = b$ :

$$\begin{bmatrix} 1 & 1 & 2 \\ 1 & 1 & 2 \\ 2 & 2 & 2 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} 2 \\ 2 \\ 4 \end{bmatrix}$$

- (a) (5 %) Find the general (complete) solution?  
 (b) (5 %) Find a basis for the column space of the 3 by 9 block matrix  $[A \ 2A \ A^2]$ .

3. Please construct 3 by 3 matrices  $A$  and  $B$  with these properties:

- (a) (5 %)  $A$  is a symmetric matrix. Its row space is spanned by the vector  $(1, 1, 2)$  and its column space is spanned by the vector  $(2, 2, 4)$ .  
 (b) (5 %) All three of these equations have no solution but  $B \neq 0$ :

$$Bx = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}, \quad Bx = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix}, \quad Bx = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}.$$

4. Suppose the single value decomposition  $SVD \ A = UEV^T$  is

$$A = \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} 9 & 0 \\ 0 & 4 \end{bmatrix} \begin{bmatrix} \cos \alpha & \sin \alpha \\ -\sin \alpha & \cos \alpha \end{bmatrix}$$

- (a) (5 %) For which angles  $\theta$  and  $\alpha$  ( $0$  to  $\pi/2$ ) is  $A$  a positive definite symmetric matrix?  
 (b) (5 %) What are the eigenvalues and eigenvectors of  $A^T A$ ?



5. (a) (20%) Find the eigenvalues and a set of orthonormal eigenvectors for

$$P = \begin{bmatrix} 1 & 2 & 3 \\ 2 & 4 & 6 \\ 3 & 6 & 9 \end{bmatrix}$$

(b) (10%) Find the maximum value of

$$\frac{x^T P x}{x^T x}$$

where  $x$  is any nonzero  $3 \times 1$  real vector.

6. (10%) Find the rank of

$$B = \begin{bmatrix} 2 & -1 & 4 & 1 & 3 \\ 6 & 0 & 0 & 1 & 5 \\ 1 & 5 & 2 & 1 & 1 \\ 2 & 2 & 3 & 5 & 5 \\ 5 & 4 & 7 & 10 & 11 \end{bmatrix}$$

Note: You must show the derivation procedure.

7. (10%) Prove that the eigenvectors of a symmetric matrix corresponding to distinct eigenvalues are orthogonal.



1. Suppose we have a processor with a base CPI of 2.5, assuming all references hit in the primary cache, and a clock rate of 200 MHz. Assume a main memory access time of 200 ns, including the miss handling. Suppose the miss rate per instruction at the primary cache is 10%.
  - (a) What is the CPI in this system which has a primary cache(10%)
  - (b) same as (a), but we add a secondary cache that has a 40-ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 5%. In this situation, what is the CPI (10%)
  
2. A computer system has 32 address lines and 16-Kbyte cache. Each cache block size is 32-byte. For the following cases,
  - (i) A direct mapped cache,
  - (ii) A fully associative cache,
  - (iii) A 4-way set associative cache,
  - (a) how many comparators are required in each cases?(6%)
  - (b) when the CPU references an address 0xABCDEF12, what is the tag value for each cases? (6%)
  
3. In a big-endian CPU, when the CPU stores the value 0x1A2B3C4D into memory address 0x1000. What is the content of the memory address 0x1002? (5%)
  
4. The number of clock cycles for each instruction class is the following: loads: 6, stores: 5, ALU instructions: 4, Branches: 3, and Jumps:4. Assume the gcc instruction mix is 25% loads, 10% stores, 20% branches, 5% jumps, and 40% ALU. What is the CPI? (8%)
  
5. Consider a program consisting of 200 lw instructions and in which each instruction is independent upon the instruction before it. What would the actual CPI be if the program were run on the 6-stage pipelined datapath? (5%)



6. In the IEEE-754 floating-point standard the value of a single-precision number  
 $X = (-1)^S \times (1.F) \times 2^{E-127}$ .

(a) Convert the decimal number 123.6875 to a 32-bit floating-point number with IEEE 754 format. (5%)

(b) What is the decimal value of the number shown in the following table : (5%)

S	E	F
1	10000101	10 1000 000000000000 0000 0

7. What is bus arbitration? Please list four classes of scheme for bus arbitration. (10%)

8. Please draw the block diagram of BCD adder. (8%)

9. What is pipeline stall in a processor? Briefly explain three factors that can cause pipeline stall. (8%)

10. You are trying to decide which system to purchase and are considering two different computers M1 and M2 :

Instruction Class	CPI for M1	CPI for M2
A	4	2
B	6	4
C	8	3

The machine M1 has a clock rate of 1GHz and M2 has a clock rate of 500MHz.

- (a) If the number of instructions executed in a certain program is divided equally among the cases of instructions, how much faster is M2 than M1? (5%)

- (b) Consider the three compilers C1, C2, and C3 that produce the frequency results shown below :

Instruction Class	C1	C2	C3
A	30%	30%	50%
B	50%	20%	30%
C	20%	50%	20%

For compiler C1, compare M1 and M2. Which processor is faster and by how much? (5%)

- (c) Assuming that any of the three compilers can be used on M1 or M2, Which of these two machines and which compiler should be purchased? (4%)



1. Determine the electron and hole densities in a silicon substrate at 25 °C containing  $5.0 \times 10^{15}$  boron atoms/cm<sup>3</sup> and  $4.0 \times 10^{17}$  phosphorus atoms/cm<sup>3</sup>. (15%)
2. Describe briefly the fabrication process sequence of a silicon enhancement-mode P-channel MOSFET using the planar IC technology. (20%)
3. Construct a 2-bit shift register using J-K master-slave FLIP-FLOPs. (15%)
4. (1) Figure 1(a) shows the NMOS depletion-load inverter, where  $V_{ThD} = 1.0V$ ,  $V_{ThL} = -2.0V$ , and  $k_{nD} / k_{nL} = 4$ . If  $V_i = 0.2V$  find  $V_o$ . (15%)  
(2) Figure 1(b) shows the NMOS enhancement-load inverter, where the parameters of transistors Q1 and Q2 are  $V_{Th1} = V_{Th2} = 1.0V$ ,  $k_{n1}/k_{n2}=4$ , and  $V_{DD}=5V$ . If  $V_i = V_L$ , then  $V_o = V_H$ , and if  $V_i = V_H$ , then  $V_o = V_L$ . Find the values of  $V_L$  and  $V_H$ . (20%)

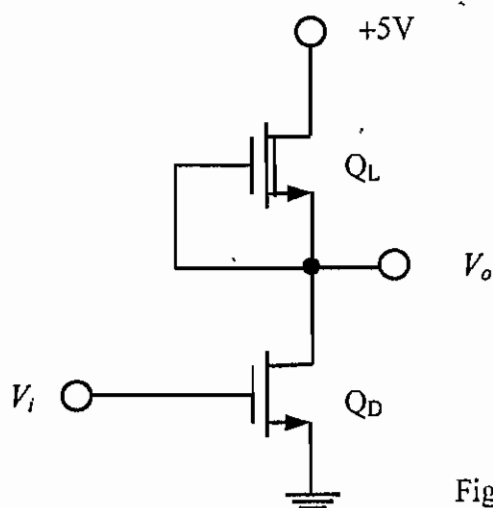


Fig. 1(a)

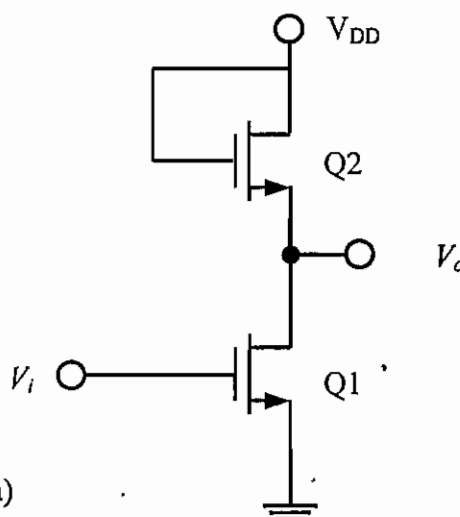


Fig. 1(b)



5. Figure 2 shows the common-emitter circuit. Find the higher 3 dB frequency and Miller capacitance, under the conditions of  $r_s = \infty$ ,  $R_1 \parallel R_2 = 5\text{k}\Omega$ ,  $I_{CQ} = 4\text{mA}$ ,  $\beta_o = 200$ ,  $\lambda = 0$ ,  $C_\mu = 5\text{pF}$ , and  $f_T = 500\text{MHz}$ . (15%)

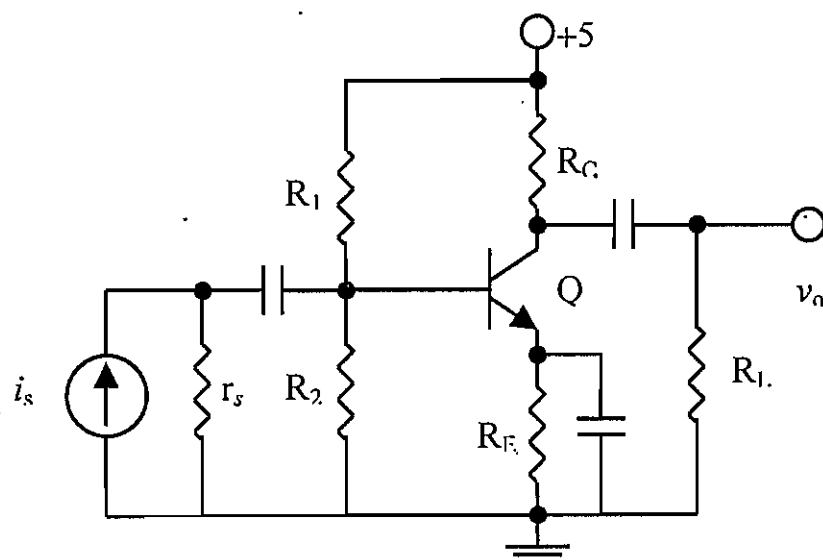
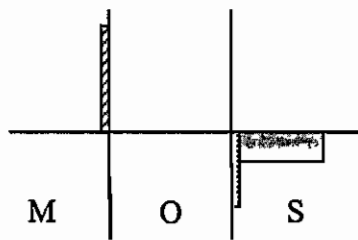


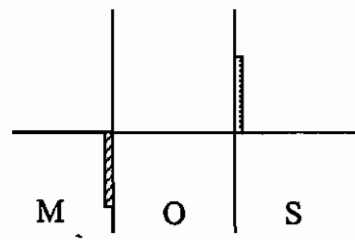
Fig.2



1. Consider 2 ideal pn junctions at  $T = 300$  K, having exactly the same electrical and physical parameters except for the bandgap energy of the semiconductor materials. The first pn junction has a bandgap energy of 0.525 eV and a forward bias current of 10 mA with  $V_a = 0.255$  V. For the second pn junction, design the bandgap energy so that a forward bias voltage of  $V_a = 0.32$  V will produce a current of 10  $\mu$ A. (20%)
2. Light is incident on a silicon sample starting at  $t = 0$  and generating excess carriers uniformly throughout the silicon for  $t > 0$ . The generating rate is  $5 \times 10^{21} \text{ cm}^{-3} \text{ sec}^{-1}$ . The silicon ( $T = 300$  K) is n-type with  $N_d = 5 \times 10^{16} \text{ cm}^{-3}$  and  $N_a = 0$ . Let  $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$ ,  $\tau_{n0} = 10^{-6}$  sec, and  $\tau_{p0} = 10^{-7}$  sec. Also let  $\mu_n = 1000 \text{ cm}^2/\text{V-sec}$  and  $\mu_p = 420 \text{ cm}^2/\text{V-sec}$ . Please determine the conductivity of the silicon as a function of time for  $t \geq 0$ . (20%)
3. For a bipolar junction transistor, (a) explain current crowding effect (5%), (b) explain the reason and result of emitter bandgap narrowing (5%), (c) explain the effect of punch-through (5%), and (d) derive the expression for the base transit time (5%).
4. The dc charge distributions of two MOS capacitors are shown in the figure. For each case, answer the following questions: (a) Is the semiconductor n-type or p-type? (6%) (b) Is the device biased in the accumulation, depletion, or inversion mode? (6%) (c) Draw the energy-band diagram through the MOS structure (6%).



(1)

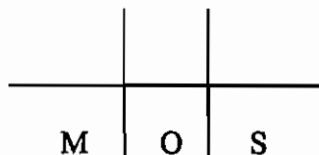


(2)

5. A MOS transistor is fabricated on a p-type silicon substrate with  $N_a = 5 \times 10^{15} \text{ cm}^{-3}$ . The oxide thickness is  $t_{\text{ox}} = 80 \text{ \AA}$  and the equivalent fixed oxide charge is  $Q'_{\text{f}} = 2 \times 10^{11}$  (electron charges/cm<sup>2</sup>). The gate is  $n^+$  polysilicon.  $T = 300$  K.
  - (a) Draw the energy band diagram in the p-type semiconductor at the threshold inversion point. Indicate the amount of surface potential in the diagram. (4%)
  - (b) Calculate the maximum space charge width. (4%)



- (c) Determine the flat-band voltage. Use the approximate Fermi level for the  $n^+$  polysilicon. (5%)
- (d) Draw the charge distribution in the MOS capacitor at flat-band. Indicate the amounts of charges. (4%)



- (e) Calculate the threshold voltage. (5%)

 B.4 Silicon, gallium arsenide, and germanium properties ( $T = 300^{\circ}\text{K}$ )

Property	Si	GaAs	Ge
Atoms ( $\text{cm}^{-3}$ )	$5.0 \times 10^{22}$	$4.42 \times 10^{22}$	$4.42 \times 10^{22}$
Atomic weight	28.09	144.63	72.60
Crystal structure	Diamond	Zincblende	Diamond
Density ( $\text{g/cm}^{-3}$ )	2.33	5.32	5.33
Lattice constant ( $\text{\AA}$ )	5.43	5.65	5.65
Melting point ( $^{\circ}\text{C}$ )	1415	1238	937
Dielectric constant	11.7	13.1	16.0
Bandgap energy (eV)	1.12	1.42	0.66
Electron affinity, $\chi$ , (volts)	4.01	4.07	4.13
Effective density of states in conduction band, $N_c$ , ( $\text{cm}^{-3}$ )	$2.8 \times 10^{19}$	$4.7 \times 10^{17}$	$1.04 \times 10^{19}$
Effective density of states in valence band, $N_v$ , ( $\text{cm}^{-3}$ )	$1.04 \times 10^{19}$	$7.0 \times 10^{18}$	$6.0 \times 10^{18}$
Intrinsic carrier concentration ( $\text{cm}^{-3}$ )	$1.5 \times 10^{10}$	$1.8 \times 10^6$	$2.4 \times 10^{13}$
Mobility ( $\text{cm}^2/\text{V-s}$ )			
Electron, $\mu_n$	1350	8500	3900
Hole, $\mu_p$	480	400	1900
Effective mass, $\left(\frac{m^*}{m_0}\right)$			
Electrons	$m_{t1}^* = 0.98$ $m_{t2}^* = 0.19$	0.067	1.64 0.082
Holes	$m_{ih}^* = 0.16$ $m_{hh}^* = 0.49$	0.082 0.45	0.044 0.28
Effective mass (density of states)			
Electrons, $\left(\frac{m_n^*}{m_0}\right)$	1.08	0.067	0.55
Holes, $\left(\frac{m_p^*}{m_0}\right)$	0.56	0.48	0.37




**B.3 Physical constants**

Avogadro's number	$N_A = 6.02 \times 10^{23}$ atoms per gram molecular weight
Boltzmann's constant	$k = 1.38 \times 10^{-23}$ J/K $= 8.62 \times 10^{-5}$ eV/K
Electronic charge (magnitude)	$e = 1.60 \times 10^{-19}$ C
Free electron rest mass	$m_0 = 9.11 \times 10^{-31}$ kg
Permeability of free space	$\mu_0 = 4\pi \times 10^{-7}$ H/m
Permittivity of free space	$\epsilon_0 = 8.85 \times 10^{-14}$ F/cm $= 8.85 \times 10^{-12}$ F/m
Planck's constant	$h = 6.625 \times 10^{-34}$ J-s $= 4.135 \times 10^{-15}$ eV-s $\frac{h}{2\pi} = \hbar = 1.054 \times 10^{-34}$ J-s
Proton rest mass	$M = 1.67 \times 10^{-27}$ kg
Speed of light in vacuum	$c = 2.998 \times 10^{10}$ cm/s
Thermal voltage ( $T = 300^\circ\text{K}$ )	$V_T = \frac{kT}{e} = 0.0259$ volt $kT = 0.0259$ eV

**B.6 Properties of  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$  ( $T = 300^\circ\text{K}$ )**

Property	$\text{SiO}_2$	$\text{Si}_3\text{N}_4$
Crystal structure	[Amorphous for most integrated circuit applications]	
Atomic or molecular density ( $\text{cm}^{-3}$ )	$2.2 \times 10^{22}$	$1.48 \times 10^{22}$
Density ( $\text{g}\cdot\text{cm}^{-3}$ )	2.2	3.4
Energy gap	$\approx 9$ eV	4.7 eV
Dielectric constant	3.9	7.5
Melting point ( $^\circ\text{C}$ )	$\approx 1700$	$\approx 1900$

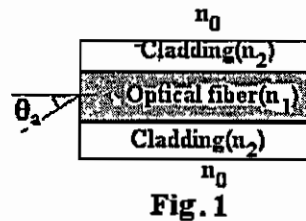


說明：本試卷共六大題，總分共計100分。

- (20%) 1. Questions:
- What is the physical significance of the equation of continuity? (4%)
  - Explain the Hall effect? (4%)
  - Explain the significance of displacement current. (4%)
  - When does the critical angle exist at an interface of two nonmagnetic media? (4%)
  - Explain the principle of electrostatic shielding. (4%)
- (15%) 2. Determine the capacitance of an isolated conducting sphere of radius  $a$  that is coated with a dielectric layer of uniform thickness  $d$ . The dielectric has an electric susceptibility  $\chi_e$ .
- (20%) 3. A dielectric sphere of radius  $a$  and dielectric constant  $\epsilon_r$  is placed in an initially uniform electric field,  $\mathbf{E}_0 = \mathbf{a}_z E_0$ , in air. Determine  $V(R, \theta)$  inside and outside the dielectric sphere, and the polarization vector  $\mathbf{P}$  of this sphere, where  $R$  is the distance from the origin and  $\theta$  is the angle between the  $z$ -axis and the radius vector.
- (15%) 4. Consider a plane boundary ( $y=0$ ) between air (region 1,  $\mu_{r1} = 1$ ) and iron (region 2,  $\mu_{r2} = 5000$ ). Assuming  $\mathbf{B}_1 = \mathbf{a}_x 0.5 - \mathbf{a}_y 10$  (mT), find (a)  $\mathbf{B}_2$  (8%) and (b) the angle that  $\mathbf{B}_2$  makes with the interface. (7%)
- (15%) 5. Electric currents  $I$  flow in opposite directions along two straight, parallel conducting wires of infinite length. The distances between a point  $P$  in space and the two conducting wires are  $r_1$  and  $r_2$ , respectively. Determine the magnetic vector potential at the point  $P$ .



- (15%) 6. Individual optical fibers are usually cladded by a material of a lower refractive index, as shown in Fig.1, where  $n_2 < n_1$ . Express the maximum angle of incidence  $\theta_a$  in terms of  $n_0$ ,  $n_1$ , and  $n_2$  for meridional rays incident on the core's end face to be trapped inside the core by total internal reflection. (Meridional rays are those that pass through the fiber axis.)





1. (10 points) Design a Turing machine that performs the addition of two nonnegative unary numbers that are on the tape separated by a single blank cell. You need to show the machine's instructions and state diagram. (Note: the nonnegative unary numbers 0, 1, 2 and 3 are represented as 1, 11, 111 and 1111, respectively.)
2. (10 points) Write a complete C++ program to read in two integers and then write out the greatest common divider of those two numbers. (Hint: the input and output instructions of C++ are *cin* and *cout*, respectively)
3. (10 points) A tennis tournament has  $n$  players, where  $n > 1$ . A single match involves two players. The winner of a match will play the winner of a match in the next round, where losers are eliminated from the tournament. The two players who have won all previous rounds play the final game, and the winner wins the tournament. What is the total number of matches needed to determine the winner? Write a C++ function, named *int NumberOfMatches ( int numberOfPlyers )*, to perform this task.
4. (10 points) The following four requests could come into an operating system as it is running on a computer system: (a) the clock inside the computer has just "ticked," and we need to update the seconds counter. (b) the program running on processor  $k$  is trying to perform an illegal operation code. (c) Someone pulled the plug on the power supply; and the system will run out of power in the  $50msec$ . (d) the disk has just read the character that passed under the read/write head, and it wants to store it in memory before the next one arrives. In what order should the operating system handle these requests?
5. (10 points) Insert the keys, in the order given as follows, to build them into an AVL tree: *AZBYCX*. (Note: show the procedure step-by-step.)
6. (10 points) Construct a context-free grammar over  $\{a, b\}$  whose language contains precisely the strings with the same number of  $a$ 's and  $b$ 's.
7. (15 points) State the Church-Turing Thesis. Why is this called a thesis, instead of a theorem? Give two reasons to support the Church-Turing Thesis.



8. (10 points) What is a perceptron? Describe its algorithm. What problems can a perceptron solve? What problems cannot be solved by a perceptron? Suggest a modification to the perceptron so that the originally unsolved problems become solvable.
  
9. (15 point) The bin-packing problem follows: Given an unlimited number of bins of volume 1 unit, and given  $n$  objects, all of volume between 0.0 and 1.0, find the minimum number of bins needed to store the  $n$  objects. Describe a brute-force algorithm, an approximation algorithm and an optimal algorithm to solve the problem. Give an example to demonstrate your algorithms. What are their time complexities?



題目1至題目10為多選題，每題5分。每題需全部答對才給分，答錯倒扣1.5分。

1. Which events can cause a trap (or software interrupt)?
  - (A) division by zero
  - (B) I/O completion
  - (C) clock interrupt
  - (D) system call
  
2. Which are correct for DMA?
  - (A) While the DMA controller is performing the data transfer, the CPU waits for its completion.
  - (B) It is used for high-speed I/O devices.
  - (C) Only one interrupt is generated per block.
  - (D) The DMA controller steals memory cycles from the CPU.
  
3. Which schedulers can be used to control the degree of multiprogramming?
  - (A) job scheduler
  - (B) CPU scheduler
  - (C) medium-term scheduler
  - (D) disk scheduler
  
4. Which are correct for indirect communication (or mailboxes)?
  - (A) A process that wants to communication must explicitly name the recipient or sender of the communication.
  - (B) A link is associated with exactly two processes.
  - (C) A number of different links may exist between each pair of communicating processes.
  - (D) A link is established between a pair of processes only if both members of the pair have a shared mailbox.
  
5. Which are correct for multithreading?
  - (A) A traditional process has a single thread of control.
  - (B) A thread comprises a thread ID, a program counter, a register set, a stack, and its data section.
  - (C) Windows 2000 implements the one-to-one multithreading model.
  - (D) Solaris 2 supports the many-to-many multithreading model.



6. Which scheduling criteria can be used to compare CPU-scheduling algorithms?
- (A) waiting time
  - (B) turnaround time
  - (C) I/O access time
  - (D) response time
7. For deadlock prevention that a process requests all needed resources prior to commencement of execution, what conditions does the approach try to prevent?
- (A) mutual exclusion
  - (B) hold and wait
  - (C) no preemption
  - (D) circular wait
8. In a paging system using TLB, if it takes 20 ns to search TLB, and 100 ns to access memory, then under what hit ratios the effective memory-access time will be less than or equal to 140 ns?
- (A) 0.9
  - (B) 0.85
  - (C) 0.8
  - (D) 0.75
9. Which are correct for page sizes?
- (A) Because each active process must have its own copy of the page table, a small page size is desirable.
  - (B) To minimize internal fragmentation, we need a small page size.
  - (C) A desire to minimize I/O time argues for a large page size.
  - (D) With a larger page size, locality will be improved.
10. Which are correct for disk space allocations such as contiguous, linked, and indexed?
- (A) One problem with contiguous allocation is determining how much space is needed for a file.
  - (B) There is no external fragmentation with linked allocation.
  - (C) It is inefficient to support a direct-access capability for linked allocation files.
  - (D) Indexed allocation supports direct access, without suffering from external fragmentation.



11. Compare and contrast the two terms regarding name mapping in a distributed file system: location transparency and location independence. (10%)

12. FIFO page replacement is relatively easy to implement, and has low overhead. But FIFO can easily replace a heavily used page. Design a simple modification to FIFO that is also easy to implement, has low overhead, and prevents a heavily used page from being replaced. (15%)

13. What is "address binding"? List three "binding time". (10%)

14. The following code is a shared-memory solution to the bounded-buffer problem. The producer and consumer processes share the following variables:

**Var** *n*;

**Type** *item*=...;

**Var** *buffer*: array [0..*n*-1] of *item*;

*in*, *out*: 0..*n*-1; /\* *in* and *out* are initialized to the value 0\*/

The code allows at most *n*-1 items in the buffer at the same time. Modify the code to allow all the buffers to be utilized fully. (15%)

**PRODUCER process:**

**repeat**

...

produce an *item* in *nextp*

...

**while** *in*+1 mod *n* = *out* do *no-op*;

*buffer*[*in*]:=*nextp*;

*in*:=*in*+1 mod *n*;

**until** *false*;

**CONSUMER process:**

**repeat**

**while** *in* = *out* do *no-op*;

*nextc*:=*buffer*[*out*];

*out* := *out*+1 mod *n*;

...

consume the *item* in *nextc*

...

**until** *false*;