國立雲林科技大學　系所：電資所
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計算題共六題

1. (20%) An inverting amplifier with nominal gain of –20 V/V employs an op amp having a dc gain of 10^4 and a unity-gain frequency of 10^6 Hz.
   a. What is the 3-dB frequency f_{3dB} of the closed-loop amplifier? (10%)
   b. What is its gain at 0.1 f_{3dB} and at 10 f_{3dB} ?(10%)

2. (20%) A BJT for which breakdown voltage BV_{CBO} is 30V is connected as shown in Fig. 1. What voltages would you measure on the collector, base, and emitter?

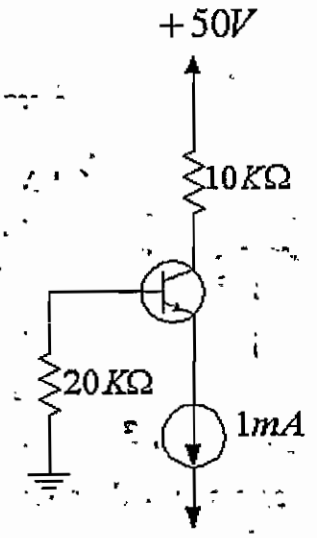

Fig. 1

3. (10%) Design the MOS differential amplifier of Fig. 2 to operate at $V_{GS} - V_t = 0.2$V and to provide a transconductance g_m of 1mA/V. Specify the W/L ratios and the bias current. The technology available provides $V_t = 0.8$V and $\mu_n C_{ox} = 90\mu$ A/V^2.

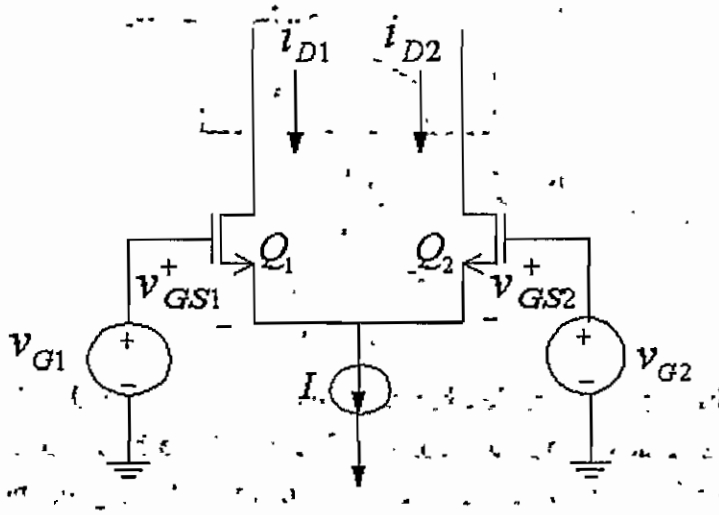

Fig. 2

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4. (20%) For the circuit shown in Fig. 3, if the nMOS transistor has parameters of $V_t = 2$ V and $\mu_n C_{ox} \frac{W}{L} = 0.5\ mA/V^2$, please use the feedback-analysis method to find the following values.

   a. Voltage gain (V_O/V_S) (10%)

   b. Input resistance R_{in} (5%)

   c. Output resistance R_{out} (5%)

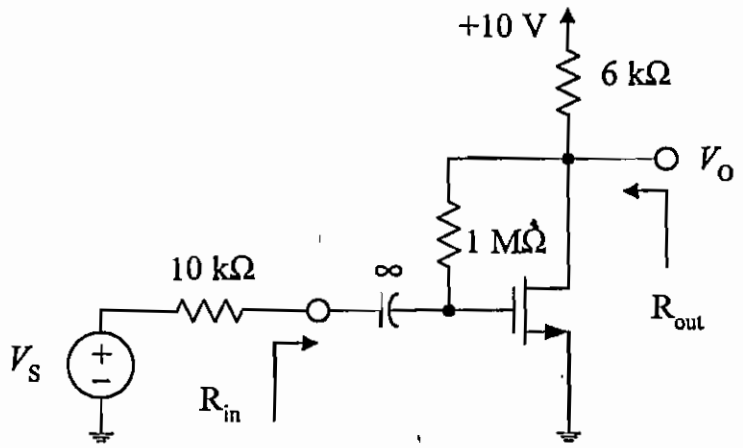

Fig. 3

5. (20%) Fig. 4 shows a filter circuit assuming that the op amp is ideal.

   a. Please derive the transfer function of the filter circuit. (10%)

   b. Use $C_1 = C_2 = 10\ nF$ to design the circuit for a maximally flat response with a 3-dB frequency of 10^3 rad/s (10%).

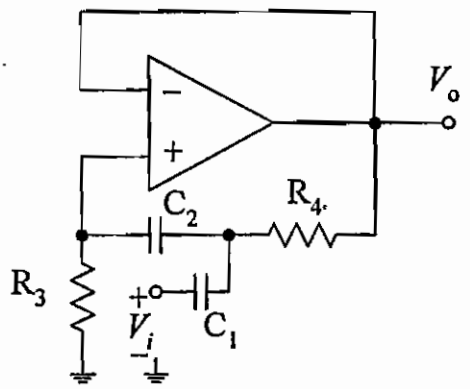

Fig. 4

6. (10%) A BJT differential amplifier, biased to have $r_e = 50\ \Omega$ and utilizing two 100-Ω emitter resistors and 5-kΩ loads, drives a second differential stage biased to have $r_e = 20\ \Omega$. Assume that all BJTs have $\beta = 150$. What are the values of the voltage gain and input resistance of the first stage? (Note: You need to draw the corresponding amplifier circuit in your answer.)

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1. (6%) Which of the following statements are always true?
   (a) *If* $A+B=C$, *then* $A\overline{D}+B\overline{D}=C\overline{D}$.
   (b) *If* $\overline{A}B+\overline{A}C=\overline{A}D$, *then* $B+C=D$.
   (c) *If* $A+B=C$, *then* $A+B+D=C+D$.
   (d) *If* $A+B+C=C+D$, *then* $A+B=D$.

2. (10%) Determine which of the following equations are always valid:
   (a) $\overline{a}b+\overline{b}c+\overline{c}a=a\overline{b}+b\overline{c}+c\overline{a}$
   (b) $(a+b)(b+c)(c+a)=(\overline{a}+\overline{b})(\overline{b}+\overline{c})(\overline{c}+\overline{a})$
   (c) $abc+a\overline{b}\overline{c}+\overline{b}cd+\overline{b}\overline{c}d+ad=abc+a\overline{b}\overline{c}+\overline{b}cd+b\overline{c}d$.

3. (8%) Complete the timing diagram for the following circuit in Fig. 1. Note that the CK inputs on the two flip-flops are different.

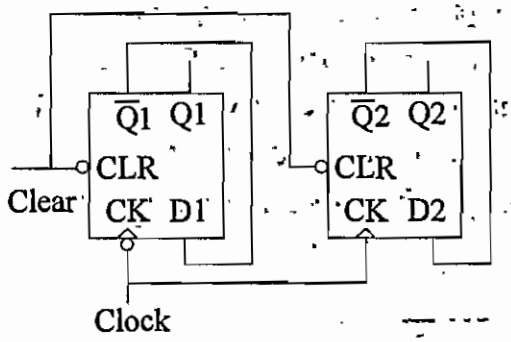

Fig. 1 (a)

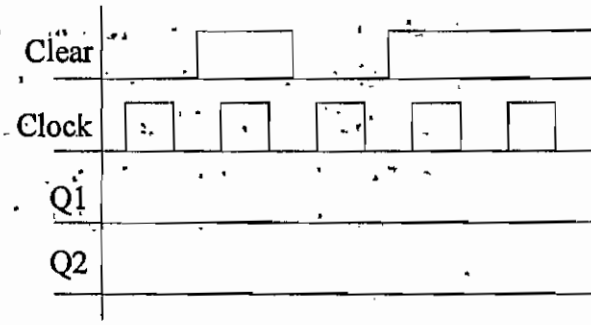

Fig. 1 (b)

4. A Mealy sequential network has 1 input, 1 output, and 2 flip-flops. A timing chart for the network is shown in Fig. 2.
   (a) (10%) Construct a state table and state graph for the network.
   (b) (10%) Using D flip-flops, design the logic circuit.

Fig. 2

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5. (6%) Reduce the following state table to a minimum number of states.

Table 1

Present State	Next State		Present Output (Z)
	X = 0	1	
a	f	d	0
b	d	a	1
c	h	b	0
d	b	c	1
e	g	b	0
f	a	h	0
g	e	c	0
h	c	f	0

6. (12%) Assume the memory map of a microprocessor system is as shown in Fig. 3. Each instruction is 2-word long. The first word contains the OP code and the addressing mode. The second word contains the address (ADRS) or the literal (LIT). Subject to Table 2, please calculate the effective address of the operand and determine the content of register AC to fill out the entries in the table. Note: LDA means load to register AC and PC is the program counter.

PC = 250

R1 = 400

AC

	Memory	
250	OP code	Mode
251	500	
252	Next instruction	
⋮	⋮	
400	700	
⋮	⋮	
500	800	
⋮	⋮	
752	600	
⋮	⋮	
800	300	
⋮	⋮	
900	200	
⋮	⋮	

Fig. 3.

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Table 2

Addressing mode	Instruction	Effective address	Content of AC
Direct	LDA ADRS		
Immediate	LDA #NBR		
Indirect	LDA [ADRS]		
Relative	LDA $ADRS		
Index	LDA ADRS (R1)		
Register indirect	LDA (R1)		

7. (13%) In whatever assembly language you are familiar with, write a subroutine DIVIT to perform the function X = Y/Z. Assume the division instruction "DIVS DX, RX" is available as shown in Figure 4. The subroutine passes the arguments using pointer A0. The argument list is 10-byte long and organized as shown in Fig. 4. For clarity, please comment on every assembly instruction you write down.

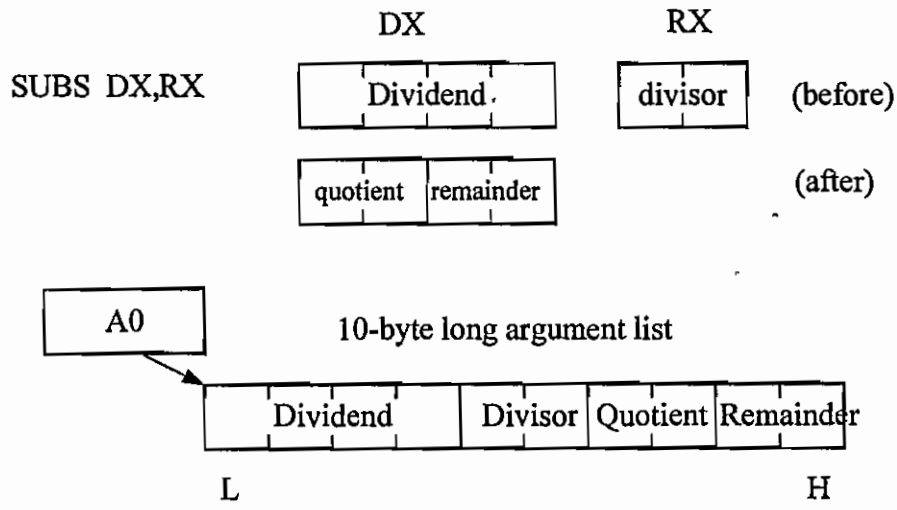

Fig. 4

8. Consider a computer with 32-bit addressing, a 512 KB cache and the block size is 16-byte wide.

(a) (6%) How many bits are there in the tag entry?

1. a direct map cache
2. a fully associative cache
3. a 4-way set associative cache

(b) (6%) Please describe three cache line replacement algorithm

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9. Please draw the block diagram of a pipelined processor with the following features

(a) (8%) two parallel data memories (RAMs), one program memory (ROM), an ALU, a multiplier, a register file and two auxiliary address register units (AARU)

(b) (5%) In your designs, how many cycles are required to complete one instruction and what are the operations performed in these cycles?

Note: AARU is a function unit to decode the instruction and calculate the effective addresses of the operands

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1. (12%) Fing all values of a for which $\{[a^2 \quad 0 \quad 1],[0 \quad a \quad 2],[1 \quad 0 \quad 1]\}$ is a basis for R_3.

2. (13%) Let V be R_3 and let $S=\{v_1, v_2, v_3\}$ and $T=\{w_1, w_2, w_3\}$ be ordered bases for R_3, where

$$v_1=\begin{bmatrix}2\\0\\1\end{bmatrix},\ v_2=\begin{bmatrix}1\\2\\0\end{bmatrix},\ v_3=\begin{bmatrix}1\\1\\1\end{bmatrix} \text{ and } w_1=\begin{bmatrix}6\\3\\3\end{bmatrix},\ w_2=\begin{bmatrix}4\\-1\\3\end{bmatrix},\ w_3=\begin{bmatrix}5\\5\\2\end{bmatrix}.$$

Compute the transition matrix $P_{S\leftarrow T}$ from the T-basis to the S-basis.

3. (12%) Let $L: R^3 \to R^2$ be a linear transformation for which we know that

$$L\left(\begin{bmatrix}1\\0\\0\end{bmatrix}\right)=\begin{bmatrix}2\\-4\end{bmatrix},\ L\left(\begin{bmatrix}0\\1\\0\end{bmatrix}\right)=\begin{bmatrix}3\\-5\end{bmatrix},\ L\left(\begin{bmatrix}0\\0\\1\end{bmatrix}\right)=\begin{bmatrix}2\\3\end{bmatrix}.$$

What is $L\left(\begin{bmatrix}1\\-2\\3\end{bmatrix}\right)$?

4. (13%) Let L be the counterclockwise rotation through $60°$. If T is the triangle with vertices (1, 1), (-3, -3), and (2, -1). Find the coordinates of the vertices of the image of T under L.

5. (10%) Find the rank of

$$A=\begin{bmatrix}1&2&3&4&5\\1&0&0&1&0\\1&1&1&1&1\\2&2&3&5&5\\5&5&7&11&11\end{bmatrix}$$

Note: You must show how you obtained your result.

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6. (20%) A matrix B is given by

$$B=\begin{bmatrix}1 & 0\\ 1 & 2\end{bmatrix}$$

Find B^{30}.

7. (20%) Consider the linear system of differential equations

$$\begin{bmatrix}x_1'\\ x_2'\\ x_3'\end{bmatrix}=\begin{bmatrix}1 & 0 & 0\\ 0 & -2 & 1\\ 0 & 0 & 3\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix}$$

Find the solution to the initial value problem determined by the initial conditions $x_1(0)=1$, $x_2(0)=5$, and $x_3(0)=10$.

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1. Suppose we have a Simplified Instructional Computer (SIC) with instruction format, addressing mode, and part of instructions listed in Fig. 1. SIC has 5 registers, A (accumulator), X (index register), L (linkage register for subroutine call), PC (program counter), and SW (status word), each with 3-byte length. Please assemble the following SIC source program to the corresponding **object program**. The answer must also include the **memory location** allocated to the object code and the **symbol table** used in the assembling process. (16%)

```
SUM     START   4000
FIRST   LDX     ZERO
        LDA     ZERO
LOOP    ADD     TABLE, X
        TIX     COUNT
        JLT     LOOP
        STA     TOTAL
        RSUB
TABLE   RESW    2000    ;two thousand words
COUNT   RESW    1
ZERO    WORD    0
TOTAL   RESW    1
        END     FIRST
```

Instruction Format

Opcode (8 bits)	x (1 bit)	Address (15 bits)

Addressing modes (TA: Target Address)
Direct x=0 TA=address
Indirect x=1 TA=address+(X)

Mnemonic	Length (byte)	Opcode	Effect
ADD m	3	18	A←(A)+(m..m+2)
JLT m	3	38	PC←m if CC set to <
LDA m	3	00	A←(m..m+2)
LDX m	3	04	X←(m..m+2)
RSUB	3	4C	PC←(L)
STA m	3	0C	(m..m+2)←(A)
TIX m	3	2C	X←(X)+1; (X): (m..m+2)
RESW	-	-	Reserve word space
WORD	-	-	Declare a word-sized constant

Fig.1

2. Immediate operands and literals are both ways of specifying an operand value in a source statement. What is the difference between a literal and an immediate operand? What are the advantages and disadvantages of each? When might each be preferable to the other? Please answer briefly. (8%) (3%) (3%) (2%)

3. Consider the following fragment of assembler language: (12%)

```
CC      START   0
        EXTDEF  EE
        EXTREF  FF
AA      WORD    35
BB      EQU     AA+23-CC
DD      EQU     70
EE      EQU     DD+AA
```

Note:
1) EXTDEF names symbols, called external symbols, defined in this control section and may be used by other sections.
2) EXTREF names symbols that are used in this control section and are defined elsewhere.

Please use "relative", "absolute", or "neither" (specify one) to answer the following questions.
(1) Is AA relative, absolute, or neither?
(2) Is BB relative, absolute, or neither?
(3) Is CC relative, absolute, or neither?
(4) Is DD relative, absolute, or neither?
(5) Is EE relative, absolute, or neither?
(6) Is FF relative, absolute, or neither?

4. Suppose two jobs are being multi-programmed together. Job A uses a great deal of CPU time and performs relatively little I/O. Job B performs many I/O operations, but requires very little CPU time. Which of these two jobs should be given higher dispatching priority to improve the overall system performance? Why? (7%)

5. What are the advantages of having several different classes of interrupts, instead of just one class with flag bits to indicate the interrupt type? (7%)

6. You are going to enhance a machine, and there are two possible improvements: either make multiply instructions run four times faster than before, or make memory access instructions run two times faster than before. You repeatedly run a program that takes 100 seconds to execute. Of this time, 20% is used for multiplication, 50% for memory access instructions, and 30% for other tasks. (12%)
   - What will the speedup be if you improve only multiplication?
   - What will the speedup be if you improve only memory access?
   - What will the speedup be if both improvements are made?

7. Assume that the time delay through each 1-bit adder is 3T. Calculate the time of adding four 4-bit numbers to the organization at the top versus the organization in the bottom in Fig. 2. (6%)

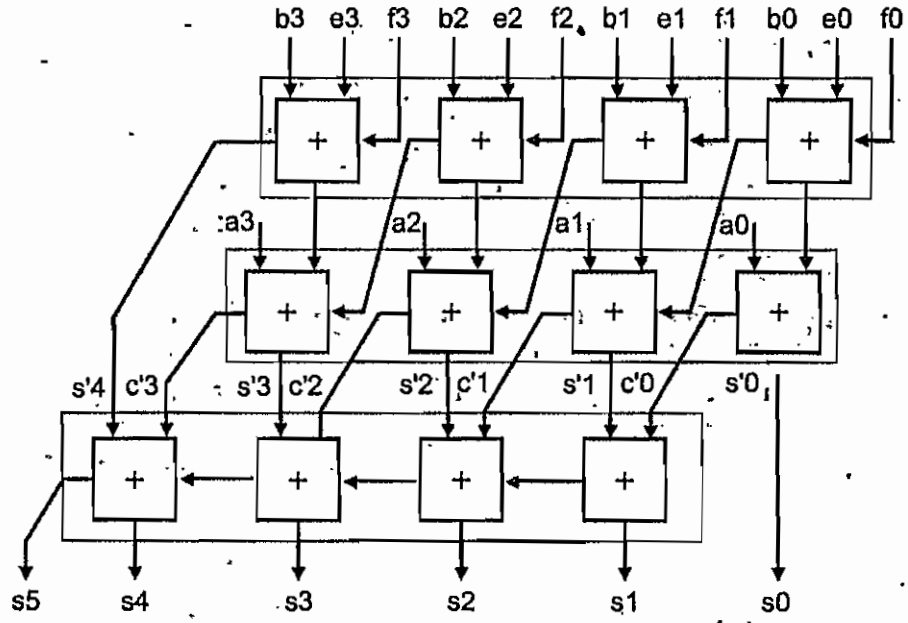

Fig. 2.

8. A CPU designs with pipeline technique. For pipelined execution, assume that half of the load instructions incur the data hazards (required one clock stall), that the one-quarter of the branches have control hazards (required one clock for branch delay). If one program has 20% loads, 15% stores, 20% branches, 5% jumps, and 40% ALU. What is the average CPI? (8%)

9. A computer system has 32 address lines and 16-Kbyte cache. Each cache block size is 32-byte. For the following cases, how many tag-bit is required for each cache block? (12%)
   - A direct mapped cache
   - A fully associative cache
   - A 4-way set associative cache

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10. Fig. 3 is a circuit which use four 4-bit carry look ahead to form a 16-bit adder (16-bit carry look ahead adder, CLA). At the same time, we can use four 16-bit CLA to build a 64-bit CLA. Assume each logic gate delay time is 1ns in the CLA circuit. (12%)
    (a) What is the maximum delay time for 4-bit CLA?)
    (b) What is the maximum delay time for 16-bit CLA?
    (c) What is the maximum delay time for 64-bit CLA?

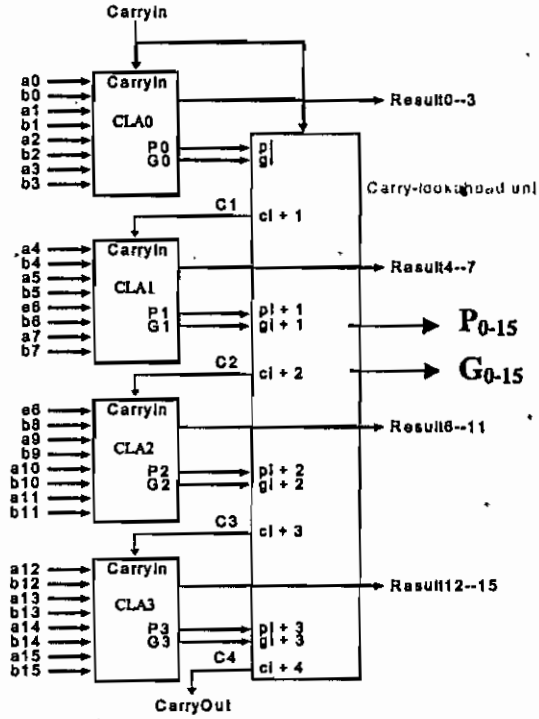

Fig. 3. Four 4-bit CLA to form a 16-bit CLA

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系所：電資所
科目：計算機概論 (乙)

1. For the following priority queue representations with n elements, give the time complexity of insertions and deletions acting on them (10%).

Representation	Insertion	Deletion
Unordered array		
Unordered linked list		
Sorted array		
Sorted linked list		
Max heap		

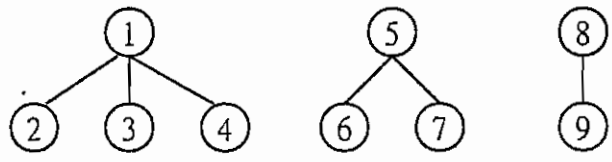
2. For an array A to store data in a row-major order, if A[0,0] is the first element in the array, and the locations of A[2,3] and A[4,7] are 1652 and 1678 respectively, what is the location of A[5,4] (10%)?

3. Fill the blanks in the following functions list-insert and list-delete acting on a doubly linked list L where x is the element to be inserted or deleted (10%).

```
list-insert(L, x)
{ next[x] ← head[L]
  if head[L]≠NIL
      then _____;
  head[L] ← x
  _____;
}

list-delete(L, x)
{ if prev[x]≠NIL
      then _____;
      else head[L] ← next[x]
  if next[x]≠NIL
      then _____;
}
```

4. Transform the following forest into a binary tree in sequence (10%).



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5. Use linear probing hashing to store the numbers 23, 30, 41, 49, 53, 60, 67 in sequence into a 7-slot hash table. The hash function used here is with the division method h(k)=k mod m. Show the contents of the 7 slots in the hash table (10%).

6. (a)Explain the member accessibility for the terms private, protected and public used in object-oriented languages. (10%)

(b)Point out and explain the errors in the following codes. (10%)

```
Class A {public: f1(a, b) {x=x+a; y=y+b;}
                 f2(a, b) {x=a; y=b;}
                 A() {f3();}
          protected: void f3();
          private: int x, y;
        };

int main() { A obj;
             obj.f2(0, 0);
             obj.f3();
             obj.x=5;
           }
```

7. (a)Explain under what situation does a computer receive two ARP replies for a single ARP request. (5%)

(b)Given an IP address and its subnet mask. Explain how to decide the number of bits of the IP address used to denote its network ID, subnet ID and host ID. (10%)

8. (a)Give an example to explain the term "tautology expression". (5%)

(b)Show how two 2-to-1 multiplexers can be connected to form a 3-to-1 multiplexer without any additional gate. (10%)

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1. Sketch the circuit configuration and the low-frequency equivalent circuit of a CMOS amplifier stage. **(20%)**

2. Describe the photolithography process used in the IC fabrication. **(15%)**

3. Sketch the logic diagram of an integrated 2-bit full adder. **(15%)**

4. The I-V measurements of a MOSFET are listed in the following table. The channel length and channel width are equal to about 1.2μm and 3.6μm, respectively. Find the threshold voltage, transconductance parameter and channel-length modulation parameter of this MOSFET. **(15%)**

V_{GS} (V)	V_{DS} (V)	I_{DS}
5	6	5.52mA
4	4	297μA
4	1	150μA
3	3	129μA
3	1	90μA

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5. Figure 1 shows the NMOS enhancement-load inverter under the parameters of $V_{ThL} = V_{ThD} = 1.0V$, $(W/L)_L = 0.5$, $(W/L)_D = 2$, $\mu_n C_{ox} = 10\mu A/V^2$, $2\phi_f = 0.7V$, and $\gamma = 0.6V^{1/2}$.

(1) Find the NM_H and NM_L with neglection of the body effect. **(10%)**

(2) Find the modified values of V_{OH} and NM_H when the body effect is taken into account. **(10%)**

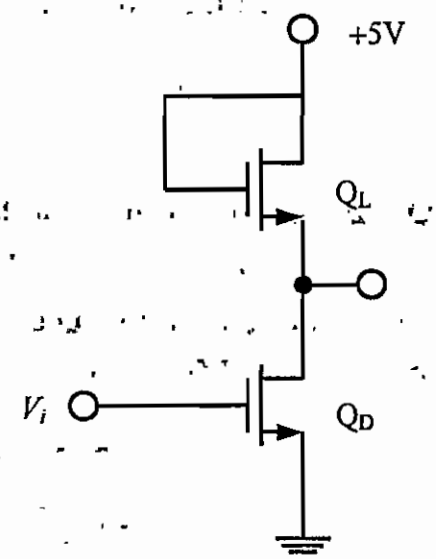

Figure 1

6. Every transistor in figure 2 has the same parameters of $V_{BE}(on) = 0.7$ V, $\beta = 120$, and $V_A = \infty$. Find the output voltage V_o and current I_Q ? **(15%)**

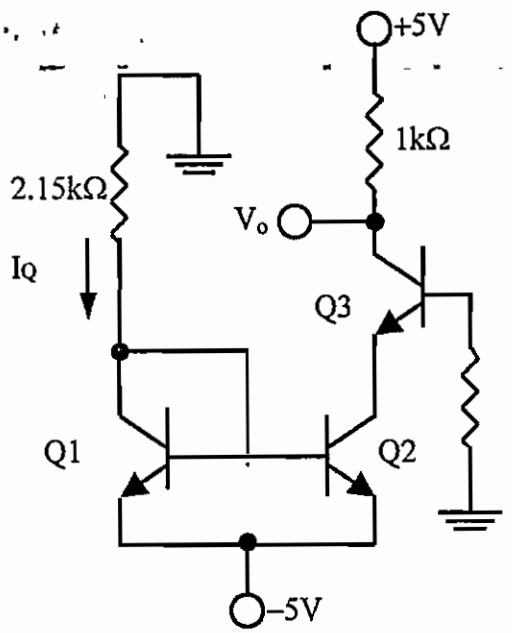

Figure 2

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系所：電資所
科目：半導體元件

1. (a) Using the parameters in Table 1, find the intrinsic carrier concentration in Ge and Si at 300 K, and also the resistivity of intrinsic Ge and Si. (10%)

	N_C (cm^{-3})	N_V (cm^{-3})	E_g (eV)	μ_n (cm^2/V-s)	μ_p (cm^2/V-s)
Ge	1.04×10^{19}	0.60×10^{19}	0.66	3900	1900
Si	2.8×10^{19}	1.04×10^{19}	1.12	1400	470

Table 1

(b) In a particular semiconductor material, the effective density of states functions are given by $N_C = N_{C0}(T)^{3/2}$ and $N_V = N_{V0}(T)^{3/2}$ where N_{C0} and N_{V0} are constants independent of temperature. The experimentally determined intrinsic carrier concentrations as a function of temperature are given in Table 2. Determine the product $N_{C0}N_{V0}$ and the bandgap energy E_g. (Assume E_g is independent of temperature.) (10%)

T (K)	n_i (cm^{-3})
200	1.84×10^{2}
300	5.85×10^{7}

Table 2

2. A silicon pn junction is to be designed to meet the following specification at 300 K. At a reversed-bias voltage of 1.2 volts, 10 percent of the total space charge region is to be in the n-region and the total junction capacitance is to be 3.5×10^{-12} F with a cross-section area of 5.5×10^{-4} cm^2. Please determine (a) N_a, (b) N_d, and (c) V_{bi}. (20%) (6%) (6%) (8%)

3. A Schottky diode and a pn junction diode have cross-sectional areas of $A = 7\times10^{-4}$ cm^2. The reverse saturation current densities at $T = 300$ K of the Schottky diode and pn junction are 4×10^{-8} A/cm^2 and 3×10^{-12} A/cm^2, respectively. A forward bias current of 0.8 mA is required in each diode. Please (a) determine the forward-bias voltage required across each diode. (10%). (b) If the voltage from part (a) is maintained across each diode, determined the current in each diode if the temperature is increased to 400 K. (It is noted that the temperature dependence of the reverse-saturation currents need to be considered. It is also assumed that $E_g = 1.12$ eV for the pn junction diode and $\phi_{B0} = 0.82$ volt for the Schottky diode.) (10%)

4. The following currents are measured in a uniformly doped npn bipolar transistor:
$I_{nE} = 1.20$ mA $I_{pE} = 0.076$ mA $I_{nC} = 1.18$ mA
$I_R = 0.018$ mA $I_G = 0.001$ mA $I_{pc0} = 0.001$ mA
Determine (a) the emitter injection efficiency factor γ, (b) the base transport factor α_T, (c) the recombination factor δ, and (d) β. (20%)

5. The experimental characteristics of an ideal n-channel MOSFET biased in the saturation region are shown in Figure 1. If $W/L = 10$ and $t_{ox} = 450$Å, determine V_T and μ_n. (10%)

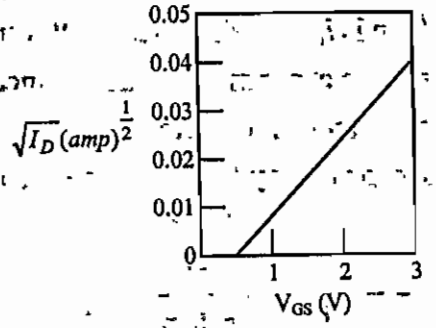

Figure 1

6. Draw an ideal low-frequency *capacitance–gate voltage* curve of a MOS capacitor with a p-type substrate. Indicate the accumulation, depletion, and inversion regions of the curve. (10%)

B.3 Physical constants

Avogadro's number	$N_A = 6.02 \times 10^{+23}$ atoms per gram molecular weight
Boltzmann's constant	$k = 1.38 \times 10^{-23}$ J/K $= 8.62 \times 10^{-5}$ eV/K
Electronic charge (magnitude)	$e = 1.60 \times 10^{-19}$ C
Free electron rest mass	$m_0 = 9.11 \times 10^{-31}$ kg
Permeability of free space	$\mu_0 = 4\pi \times 10^{-7}$ H/m
Permittivity of free space	$\epsilon_0 = 8.85 \times 10^{-14}$ F/cm $= 8.85 \times 10^{-12}$ F/m
Planck's constant	$h = 6.625 \times 10^{-34}$ J-s $= 4.135 \times 10^{-15}$ eV-s $\frac{h}{2\pi} = \hbar = 1.054 \times 10^{-34}$ J-s
Proton rest mass	$M = 1.67 \times 10^{-27}$ kg
Speed of light in vacuum	$c = 2.998 \times 10^{10}$ cm/s
Thermal voltage ($T = 300°K$)	$V_t = \frac{kT}{e} = 0.0259$ volt $kT = 0.0259$ eV

B.4 Silicon, gallium arsenide, and germanium properties ($T = 300°K$)

Property	Si	GaAs	Ge
Atoms (cm^{-3})	5.0×10^{22}	4.42×10^{22}	4.42×10^{22}
Atomic weight	28.09	144.63	72.60
Crystal structure	Diamond	Zincblende	Diamond
Density (g/cm^{-3})	2.33	5.32	5.33
Lattice constant (Å)	5.43	5.65	5.65
Melting point (°C)	1415	1238	937
Dielectric constant	11.7	13.1	16.0
Bandgap energy (eV)	1.12	1.42	0.66
Electron affinity, χ, (volts)	4.01	4.07	4.13
Effective density of states in conduction band, N_c, (cm^{-3})	2.8×10^{19}	4.7×10^{17}	1.04×10^{19}
Effective density of states in valence band, N_v, (cm^{-3})	1.04×10^{19}	7.0×10^{18}	6.0×10^{18}
Intrinsic carrier concentration (cm^{-3})	1.5×10^{10}	1.8×10^{6}	2.4×10^{13}
Mobility (cm^2/V-s)			
Electron, μ_n	1350	8500	3900
Hole, μ_p	480	400	1900
Effective mass, $\left(\frac{m^*}{m_0}\right)$			
Electrons	$m_l^* = 0.98$ $m_t^* = 0.19$	0.067	1.64 0.082
Holes	$m_{lh}^* = 0.16$ $m_{hh}^* = 0.49$	0.082 0.45	0.044 0.28
Effective mass (density of states)			
Electrons, $\left(\frac{m_n^*}{m_0}\right)$	1.08	0.067	0.55
Holes, $\left(\frac{m_p^*}{m_0}\right)$	0.56	0.48	0.37

B.6 Properties of SiO_2 and Si_3N_4 ($T = 300°K$)

Property	SiO_2	Si_3N_4
Crystal structure	[Amorphous for most integrated circuit applications]	
Atomic or molecular density (cm^{-3})	2.2×10^{22}	1.48×10^{22}
Density ($g\text{-}cm^{-3}$)	2.2	3.4
Energy gap	≈9 eV	4.7 eV
Dielectric constant	3.9	7.5
Melting point (°C)	≈1700	≈1900

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說明：本試卷共六大題，總分共計１００分。

（15分）1. Explain the following terms:
(a) The boundary conditions for electrostatic fields
(b) The boundary conditions for magnetostatic fields
(c) The boundary conditions for current density

（10分）2. Assume that the atomic nucleus may be looked upon as a uniformly charge sphere and find the maximum field strength due to this sphere. The radius of the nucleus is given by $R = 1.5\times10^{-13}\ A^{1/3}$ cm and its total charge is Ze_0, where A is the atomic weight, Z is the atomic number, and e_0 is the elementary charge.

（10分）3. Determine the system of image charges that will replace the conducting boundaries that are maintained at zero potential for an infinite line charge ρ_ℓ located midway between two large, intersecting conducting planes forming a (a) 60-degree angle, (b) 30-degree angle, as shown in Fig.1 (a) and (b), respectively.

（20分）4. A plane parallel capacitor is filled with a dielectric whose permittivity is given by $\varepsilon = \varepsilon_0(x+a)/a$, where a is the distance between the electrodes, S is the area of the plates, and the x-axis is perpendicular to the plates. Neglecting edge effects, find the capacitance C when a potential difference V is applied between the plates.

（25分）5. The cross section of a long thin metal strip and a parallel wire is shown in Fig.2. Equal and opposite current I flow in the conductors. Find the force per unit length on the conductors.

（20分）6. An electromagnetic wave in dielectric medium 1 (n_1, μ_0) impinges obliquely on a boundary plane with dielectric medium 2 (n_2, μ_0), where n_1 and n_2 are the refractive index of medium 1 and medium 2, respectively. Let θ_i and θ_t denote the incident and refraction angles, respectively, and

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use the boundary conditions for **E** and **H** to prove the following:

For perpendicular polarization,

$$\Gamma_\perp = reflection\ \ coefficient = \frac{n_1\cos\theta_i - n_2\cos\theta_t}{n_1\cos\theta_i + n_2\cos\theta_t}$$

$$t_\perp = transmission\ \ coefficient = \frac{2n_1\cos\theta_i}{n_1\cos\theta_i + n_2\cos\theta_t}$$

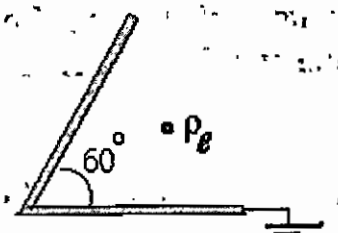

Fig.1 (a)

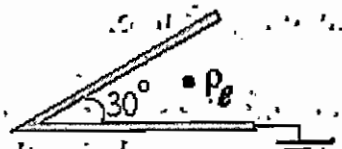

Fig.1 (b)

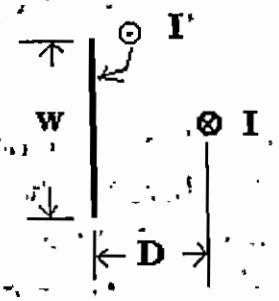

Fig.2.

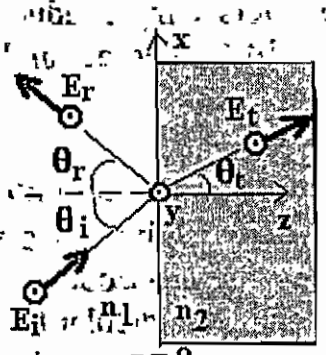

Fig.3.