國立雲林技術學院　　所別：電子與資訊工程技術研究所
八十四學年度研究所碩士班入學考試試題　　科目：工程數學

1. The linear mapping $\mathbf{L}: \mathbf{R}^3 \to \mathbf{R}^2$ defined by

$$\mathbf{L}\left(\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}\right) = \begin{bmatrix} x_1 + x_2 \\ x_2 + x_3 \end{bmatrix}$$

Let S be the subspace of $\mathbf{R}^3$ spanned by $\mathbf{e}_2 = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix}$

a. Find the $\ker(\mathbf{L})$(kernel of $\mathbf{L}$) ? and the $\mathrm{L}(\mathbf{S})$(image of S) ? (8%)

b. Find the matrix representation of $\mathbf{L}$ with respect to the orderd bases $[\mathbf{u}_1, \mathbf{u}_2, \mathbf{u}_3]$ and $[\mathbf{b}_1, \mathbf{b}_2]$ where

$$\mathbf{u}_1 = \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix}, \quad \mathbf{u}_2 = \begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix}, \quad \mathbf{u}_3 = \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix}$$

and

$$\mathbf{b}_1 = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \quad \mathbf{b}_2 = \begin{bmatrix} 1 \\ 1 \end{bmatrix} \qquad (7\%)$$

2. Let the continuous real-valued functions $\mathbf{C}[a, b]$ with inner product defined by

$$< f, g >= \int_a^b f(x)g(x)dx$$

and norm defined by

$$\|f\| = \sqrt{< f, f >}$$

Find the best least squares approximation to e^x on the internal [0, 2] by a linear function. (15%)

3. a. Let $\mathbf{A}$ be an $m \times n$ matrix. Find the nullspace of $\mathbf{A}$ if $\mathbf{A}$ has linearly independent column vectors. (10%)

b. An $n \times n$ matrix $\mathbf{B}$ is said to be idempotent if $\mathbf{B}^2 = \mathbf{B}$. Find the eigenvalues of λ for an idempotent matrix? (10%)

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4. Find a particular solution satisfying the initial condition (20%)

   a. $(2xy^2 + 2xy)dx + (x^2y + x^2)dy = 0$; $y(1) = 1$. (10%)

   b. $x^2y'' - 4xy' + 4y = x^4 + x^3$ for $x > 0$; $y(1) = 0$ and $y'(1) = 1$. (10%)

5. Solve the differential equation: $y''(t) + y'(t) - 2ty(t) = 0$. (10%)

6. Application problem. (10%)
   A 200 gallons tank is half-full of a brine in which is dissolved 50 pounds of salts. A mixture consisting of 2 pounds of salts per gallons is flowing into the tank at a rate of 10 gallons/minute, and the brine mixture in the tank is continuously stirred. Meanwhile, brine is allowed to empty out of the tank at the rate of 4 gallons /minute. What is the amount of salt in the tank at time t before the tank is filled ?

7. Solve the initial value problem (10%)

   $\dot{x}_1(t) = 3x_1(t) + 3x_2(t)$
   $\dot{x}_2(t) = x_1(t) + 5x_2(t) + 4e^{3t}$
   $x_1(0) = 1,\ x_2(0) = 0.$

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Note: There are two pages with 11 main problems. Give the answers and number them clearly.

1. What is a socket in the context of network programming? (6 pts)

2. Why is it preferable to use the lower order address bits to select the memory banks in interleaved memory systems? (4 pts)

3. Name three mechanisms for passing parameters to a subroutine module. (6 pts)

4. Consider the power consumption in a notebook computer system. What are the major components that consume most of the power? Name three components and rank their order from high to low. (6 pts)

5. The target address of a compare and branch instruction (DBEQ) is computed as follows.
Step 1: Target $\leftarrow (\text{offset}_{15})^{14}\#\#\text{offset}\#\#0^2$, condition $\leftarrow ([r_s] = [r_t])$
Step 2: If condition then PC $\leftarrow$ PC + Target, $[r_s] \leftarrow ([r_s] - 1)$
The instruction consists of the following fields: $\text{DBEQ}_{[31..26]}\#\#r_{s[25..21]}\#\#r_{t[20..16]}\#\#\text{offset}_{[15..0]}$.
Note that the program counter (PC) is incremented to point to the next instruction after an instruction is fetched. Each instruction is 32-bit long.
(a) If offset = 2, and $[r_6] = [r_8]$, which instruction will be executed after DBEQ is executed for the following sequence of instructions? (Labels are not shown.) (6 pts)

```
...
ANDI r1, r2, r3
ORI r7, r8, r4
DBEQ r6, r8, offset
ADD r7, r8, r4
NOR r7, r8, r4
OR r7, r8, r4
ADDS r7, r8, r4
ADDU r7, r8, r4
...
```

(b) Repeat (a) if offset = −1. (6 pts)
(c) If $\text{DBEQ}_{[31..26]} = 16\text{H}$, $r_s = r_t = 4$, and offset = −2, give the machine code of the DBEQ instruction in hexadecimal. (6 pts)

6. Computer Y is described as follows:
Cell size : 8 bits. Address space = 32 bits. Register size = 32 bits. Word size = 32 bits. Memory data bus size = 32 bits. Opcode size fixed (There are 50 opcodes). Number of general purpose registers = 32. Aligned fetches only. Computer Y uses an 8-bit field to specify an address mode and a register. Two bits are used to specify the size of the operand. Show the shortest possible instruction format which will add the contents of two registers and place the sum in a third register. (10 pts)

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7. (a) What is a virtual function in an object-oriented programming language (5 pts)?
(b) Write down the result of the following program (5 pts).

```
class B
{public:
virtual    char f() {return 'B';}
           char g() {return 'B';}
           char testF() {return f();}
           char testG() {return g();}
};

class D: public B
{public:
           char f() {return 'D';}
           char g() {return 'D';}
}

main()
{ D d;
print d.testF(), d.testG();
}
```

8. (a) Give the binary tree representation of the arithmetic expression A/B**C*D+E. (3 pts)
(b) Write a recursive procedure that traverses the binary tree in preorder. (4 pts)
(c) What is the prefix form of the expression shown in (a)? (3 pts)

9. Suppose that the transmitted message is 110011 with the leftmost bit transmitted first. The CRC generator pattern is 1111.
(a) Give the CRC checksum. (5 pts)
(b) What kinds of error pattern can not be caught by the CRC error detection method? (5 pts)

10. Consider the sorting problem. Explain how this problem can be solved by a divide and conquer algorithm that
(a) Divide in constant time and merge in O(n) time. (4 pts)
(b) Divide in O(n) time and merge in constant time. (4 pts)
(c) If we can divide the problem into two subproblems in equal size, what is the complexity of the above algorithms? (4 pts)

11. What do we mean when we say that an algorithm is optimal? Give an example. (8 pts)

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科目：計算機數學

* For each of the following questions, you must explain clearly how you obtain your answers in order to score points.
* Ten points for each question.

1. Suppose $T(n) = 2^n + n^4$ is the running time for a certain program, compute the tight big-oh of T(n).

2. Let B_n be the number of sequences of n digits in which no two consecutive digits are the same. Give a proof that $B_n = 10 \cdot 9^{n-1}$.

3. Draw all the simple, undirected, nonisomorphic graphs having six vertices for which the degrees of the vertices are 1, 1, 1, 2, 2, and 3.

4. Write a regular expression that defines the following language:
all strings of 0's and 1's such that the third position from the right end is 1.

5. Design a deterministic automation that correctly finds all occurrence of *man* in a character string.

6. Let $A = \begin{bmatrix} 3 & -5 \\ 1 & -3 \end{bmatrix}$. Compute A^9. (Hint: Find a matrix P such that $P^{-1}AP$ is a diagonal matrix.)

7. Maximize

$$s = 4a + 8b + 5c$$

subject to

$$a + 2b + 3c \le 18$$
$$a + 4b + c \le 6$$
$$2a + 6b + 4c \le 15$$
$$a \ge 0, \quad b \ge 0, \quad c \ge 0.$$

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Consider the conic section whose equation is

$$Q(X) = 2x^2 + 2xy + 2y^2 = 9.$$

epresent the conic section with a new coordinate system x', y' such that

$$Q'(Y) = ax'^2 + by'^2 = c.$$

hat is, find the constants a, b, and c, and express x', y' in terms of x, y.

Hint: Write $Q(x) = \begin{bmatrix} x & y \end{bmatrix} \begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix}$ and consider rotation of the conic section).

A directed graph is said to be strongly connected if for every two distinct vertices P_i nd P_j there is a path from P_i to P_j and a path from P_j to P_i. etermine whether the directed graph with the given adjacency matrix is strongly onnected.

$$\begin{bmatrix} 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix}$$

0. Find the characteristic polynomial, eigenvalues, and eigenvectors of the matrix

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ 0 & -1 & 3 & 2 \\ 0 & 0 & 3 & 3 \\ 0 & 0 & 0 & 2 \end{bmatrix}$$

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注意：1、本試題共 5 題，共 100 分。須標明題號並依序寫在答案卷上，否則不予計分。
2、書寫答案時，由第一頁起採自左而右橫寫，不得倒反。

1. Design a 4-bit circuit that can perform either BCD or binary addition under the control of a mode setting, M. When M = 0, the circuit's outputs implement binary addition. When M = 1, the outputs are BCD addition. Define all the signals that you use and describe the structure of the circuit in your design. (20%)

2. (a)What are the definitions of *static hazards* and *dynamic hazards*? (5%)

(b)Consider a two-level NAND-NAND circuit that implements the Boolean expression

$$f(A,B,C,D) = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{C}\,D + B\,C\,D + A\,B\,\overline{D}$$

Is it hazard-free in response to single-input changes? If your answer is 'yes', please show how to modify the circuit to eliminate all such hazards. If your answer is 'no', explain how you came to the conclusion that it is hazard-free.(10%)

(c)Is it possible that static logic 0-hazards may exist in a minimized *2-level sum-of-product* implementation? Justify your answer.(5%)

3. Use the tabular approach (Quine-McCluskey method) to find the minimal SOP (sum-of-product) expression for the incomplete specified four-variable function shown as follows: (20%)

$$f(A,B,C,D) = \Sigma\, m(4,5,6,8,9,10,13) + \Sigma\, d(0,7,15)$$

where *m* and *d* represent the minterm and don't-care term, respectively

4. (a)Consider the state diagram shown in Figure 1. Construct an excitation table from it by using the state assignment A = 10, B = 11, C = 01, D = 00 and JK flip-flops. (10%)

(b)Implement the excitation table and draw the resulting logic diagram. (10%)

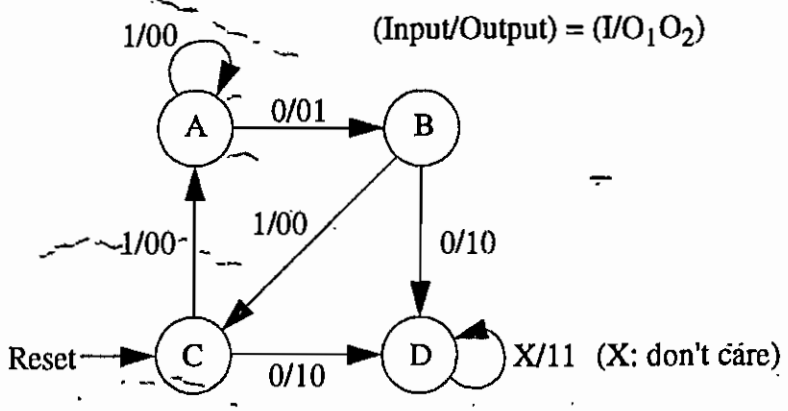

Figure 1: A four-state diagram

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科目：數位邏輯

5. (a)For the asynchronous sequential circuit shown in Figure 2, construct its corresponding flow table. The signals are defined as follows: X_1 and X_2 are asynchronous primary input variables. y_1 and y_2 are the secondary input variables and represent the 'present-state' of the circuit. Y_1 and Y_2 represent the next-state variables. (15%)

(b)Is there any critical race existing in this circuit? Justify your answer. (5%)

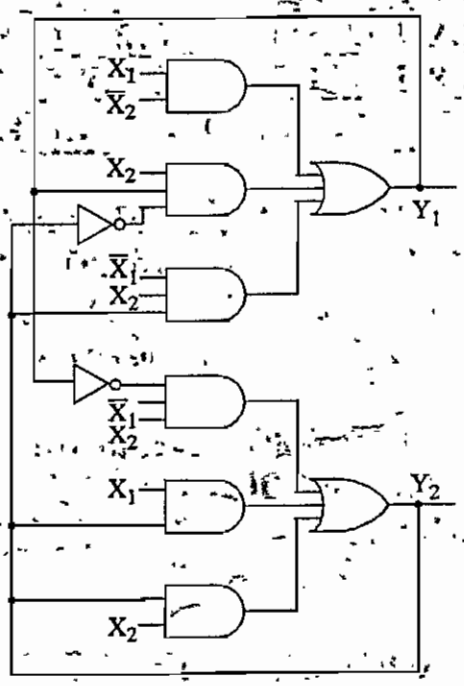

Figure 2

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注意：1. 本試題為問答題，須標明題號並依序寫在答案卷上，否則不予計分。
2. 本試題分成(a)必選題：各組考生依下列規定必須全部作答；
(b)隨選題：各組考生依下列規定任選兩題作答；

甲組：	必選題 1,2,3	隨選題 4,5,6,7,8,9
乙組：	必選題 4,5,6	隨選題 1,2,3,7,8,9
丙組：	必選題 7,8,9	隨選題 1,2,3,4,5,6

（註：每位考生共須作答五題，未依上述規定作答之題目不予計分）

1.在IC工業界中，Custom IC 就是客户委託IC公司設計符合特定功能之晶片，就您所知，目前Custom IC有那些設計技術(Design Technology)？並比較各種技術之優缺點？（可依據Chip Size, Design Cost, Performance, Power Consumption, Design Cycle 等）(20%)

2.吾人若想將一求 A,B 兩數之 GCD(Great Common Devisor) 演算方法(Algorithm)，設計成數位電路之IC晶片，應分成幾個設計步驟（可配合流程圖說明），及須應用那些種類之電腦輔助設計（軟體名稱可不寫，但功能用途須說明），請詳述之。(20%)

3.從(a)至(e)中任選三小題詳細作答(20%)
(a)試述數位電路設計成超大型積體電路(VLSI)之優缺點。
(b)何謂 Clock Skew? 其對數位電路有何影響？在設計電路時如何避免其發生。
(c)何謂 Logic Hazard（可用電路圖說明）？在設計電路時如何避免其發生。
(d)何謂 MPEG (Motion Picture Expert Group)？試畫出 MPEG Encoder系統方塊圖。
(e)何謂 HDTV (High-Definition TeleVision)? 其與傳統電視有何差異？

4. 請分析台灣的資訊產業現狀與未來發展方向. 請列舉三項分別就現狀與未來作答.(20%)

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科目：專業實務

5. 如果要將一個人電腦 PC 改造成一小型共享記憶體多處理機 (shared memory multiprocessor), 試問
   (a) 就硬體面,那些架構問題必需克服,如何克服? (10%)
   (b) 就軟體面,這個多處理機系統如何 boot 起來?(10%)

6. 試描述 Internet 之架構與管理方法.(20%)

7. (a) 目前政府正大力推動各項措施，以期在公元兩千年之際，將台灣建設成為亞太營運中心；請就此事對我國各方面可能的影響與效益，提出您個人的看法。(6%)
   (b) 您認為雲林地區適合從那些方面參與此一亞太營運中心計畫？ (7%)
   (c) 您若就讀本研究所畢業後，您個人將如何投入此一全國性的亞太營運中心計畫行列中？ (7%)

8. (a) 台灣目前的光電產業現況如何？請概述之。 (10%)
   (b) 您認為應如何促進此一產業的健全發展？ (10%)

9. (a) 請以能帶 (Energy band) 觀點，將電子材料分類。 (10%)
   (b) 請就材料特性及應用兩方面，對矽 (Si) 與砷化鎵 (GaAs) 兩種材料加以比較。 (10%)

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1 Explain the following terms
(a) **Forwarding** (short-circuiting) (10%)　　(b) **Interlock** (10%)

2. You are intended to use an **optimizing compiler** to optimize a code segment.
The code has instruction set distribution as in the following table:

Operation	Frequency	Clock cycle count
ALU ops	43%	1
Loads	21%	2
Stores	12%	2
Branches	24%	2

The optimizing compiler discards 50% of the ALU operations.
The CPU clock cycle time is **20-ns** and the instruction count is 1000.

A. Find 1) **CPI** 2.)**MIPS** and 3.) **CPU time** for the unoptimized and optimized codes. (15%)
B. Compare and explain the result you have (5%)

3. Three different machines M0, M8, and M16 that differ in their register count. All three machines have 3 operands **instructions**, and any operand can be either a memory reference or a register.
The cost of a memory operands is **6 cycles** and the cost of a register operands is one cycle. Each of the three operands has **equal probability** of being in a register.

A. What is the **cycle count** for an average instruction on each machine? (20%)
B. We now consider the **cost of restoring and saving these registers** a round procedure call. What is the answer for A if we include the additional cycles due to context switching (**0 for M0, 8 for M8 and 12 for M16**)?.(10%)

Machine	Register count	Execution cycles per operation in addition to the operands access	Probability of an operand being in a register as opposed to memory
M0	0	4	0.0
M8	8	5	0.5
M16	16	6	0.8

4. Mapping a **32-block** memory to a **8-block cache**, you use three kinds of placement policy: **fully associative, direct mapped, 2-way set associative.**
Describe graphically how you map **block 12** to the cache, using different associativities. (10%)

5. Prior to designing a cache, you would like to understand the relationship and trade-offs among such factors as **Miss rate, Miss penalty, Block size, and Average access time.**
Explain their relationship between
1.) Miss penalty v.s. block,
2.) Miss rate v.s. block size,
3.) Average access time v.s. block size,
in terms of **Hit time, Transfer time, Access time, Block-frame, Block-offset, Spatial locality, Temporal locality, Pollution point**. (20%)

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1. Consider the following fragment of SIC/XE assembler language (10%):

```
CC      START   0
        EXTDEF  EE
        EXTREF  FF
AA      WORD    35
BB      EQU     AA+23-CC
DD      EQU     70
EE      EQU     DD+AA
```

(a) Is AA relative, absolute, or neither?
(b) Is BB relative, absolute, or neither?
(c) Is CC relative, absolute, or neither?
(d) Is DD relative, absolute, or neither?
(e) Is EE relative, absolute, or neither?
(f) Is FF relative, absolute, or neither?
(g) Is 35 relative, absolute, or neither?
(h) Is AA+CC relative, absolute, or neither?
(i) Is -AA relative, absolute, or neither?
(j) Is EE-BB relative, absolute, or neither?

2. Consider an assembler and linking loader of the type described by Beck. Identify the passes of the assembler or the loader where each of the following would be done (10%):

(a) Assign relative addresses to symbols defined as labels in the program.
(b) Load the object program into memory.
(c) Assign actual addresses to program modules.
(d) Generate the object program.
(e) Detect duoble-defined entry points.
(f) Modify the relocatable portion of the object code.
(g) Enter addresses for external symbols into the external symbol table.
(h) Process EQU assembler directives.
(i) Genarate values defined in data initialization statements such as WORD and BYTE.
(j) Process the LTORG statement.

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Consider the following grammer (10%):

<asg> ::= id := <term>;
<exp> ::= id * <exp> | id * <term>;
<term> ::= id + <term> | (<exp>) | id;

Assume that the scanner will report token type id when it sees a valid Pascal identifier. Which of the following strings is a valid sentence (i.e., an <asg>) in the language generated by this grammer?

(a) ALBERT := B + C;　　(b) D := B * C;
(c) X := B + (C * D + E);　　(d) A := B + (C * D);

Describe the algorithm of a linking loader (20%).

Describe the primary objectives of three different types of schedulers, the long-term, medium-term, and short-term schedulers, and shows the possible traversal paths of jobs and programs through the schedulers (15%).

Describe Belady's anomaly, and provide an example that illustrates anomalous behavior of FIFO (15%).

In a virtual memory system, state the different effects between the following two routines. Why? (10%)

```
for (i=0;i<1000;i++)                    for (i=0;i<1000;i++)
  for (j=0;j<1000;j++)                    for (j=0;j<1000;j++)
    for (k=0;k<1000;k++)                    for (k=0;k<1000;k++)
      array[i][j][k]=1;                       array[k][j][i]=1;
```

A disk drive has 305 cylinders, four heads, and 17 sectors of 512 bytes each per track. The disk is rotated at 3000 rpm, and it has a moving-head assembly with an average head-positioning time of 30 ms. The peak data-transfer rate that the drive can sustain is 4Mbps. Calculate the average times needed to transfer 20 consecutive and 20 randomly distributed blocks (sectors) from such a disk (10%).

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科目：信號與系統

1. (20%) Given a system

$$y(t) = \int_{-\infty}^{t+2} x(\tau)d\tau$$

where $x(t)$ and $y(t)$ are the system input and output, respectively. Determine whether the system has the following properties:

(a) Time-invariance

(b) Linearity

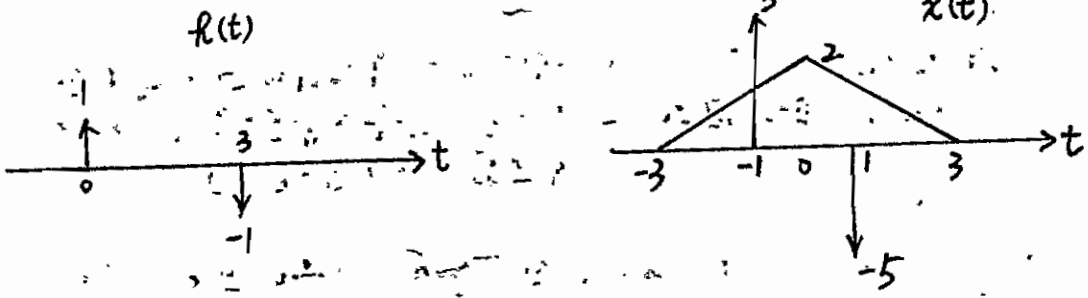
(c) Causality

(d) Stability

(e) With or without memory

You must give the correct explanation to get your credit.

2. (20%) Find the response $y(t)$ of an LTI system with impulse response $h(t)$ to the input $x(t)$, where $h(t)$ and $x(t)$ are given as



3. (20%) $H(\Omega)$ is an ideal bandpass filter given by

$$H(\Omega) = \begin{cases} A, & \Omega_a \le |\Omega| \le \Omega_b \\ 0, & \text{otherwise} \end{cases}$$

Find the impulse response of this filter.

4. (20%) How do you reconstruct a continuous-time signal $x(t)$ from its samples $x(nT)$ where T is the sampling period? Prove your answer.

5. (20%) Find the inverse Fourier transform of

$$\left[\frac{2\sin(\Omega T_1)}{\Omega}\right]^2$$

where T_1 is a constant.

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八十四學年度研究所碩士班入學考試試題　　科目：電磁學

說明：本試卷共五大題；每大題２０分；總分共計１００分。

（20分）一、在三度空間中，存在一以直角座標系統表示之電場強度

$$\vec{E} = (yz - 2x)\hat{a}_x + xz\hat{a}_y + xy\hat{a}_z$$

（6分）（a）此電場強度是否爲一靜電場？並證明之；

（7分）（b）求出此電場強度在空間中相關之電位函數？

（7分）（c）求出此電場強度相關之空間體積電荷密度值（volume charge density）？

（20分）二、有一帶電球體，其電荷對稱分佈，在下列分別之二種情況中，此球表面上的電場強度是否大於球內各點之電場強度？說明理由並證明之。

（10分）（a）電荷之體積電荷密度均勻；

（10分）（b）電荷之體積電荷密度與離開球心任一點之距離成反比。

（20分）三、已知在二同心圓球間填入導電係數（conductivity）爲常數σ_0之導體，求出此二同心圓球面（半徑分別爲 a, b；a<b）間之電阻？

（20分）四、已知一半徑 a 之圓形電流環路（circular current loop）帶有順時鐘方向之穩態電流（steady current）強度 I，利用畢歐沙瓦定律（Biot Savart's law）求出此圓形電流環路中心（圓心）處之磁通量密度（magnetic flux density）之(a)大小值（15分）與（b）方向（5分）？

（20分）五、解釋名詞

（5分）（a）焦耳定律（Joule's law）

（5分）（b）磁化向量（magnetization vector）

（5分）（c）影像電荷（image charge）

（5分）（d）向量磁位（magnetic vector potential）

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所別：機械工程技術研究所
電子與資訊工程技術研究所
科目：電子電路

1.(40%) The switch in the circuit shown in Fig.1 has been in position a for a long time. At t=0 the switch is moved to position b. What is the (a) initial value of v_c? (b) final value of v_c? (c) time constant of the circuit when the switch is in position b? (d) expression for $v_c(t)$ when $t \geq 0$?

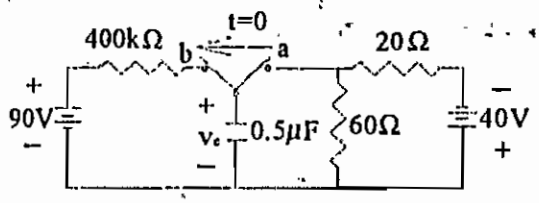

Fig.1

2.(20%) An RLC series-connected circuit is shown in Fig.2. The steady-state expression for the source voltage v_s is 750cos(5000t+30°). (a) Construct the phasor-domain equivalent circuit. (b) Calculate the steady-state current i by the phasor method.

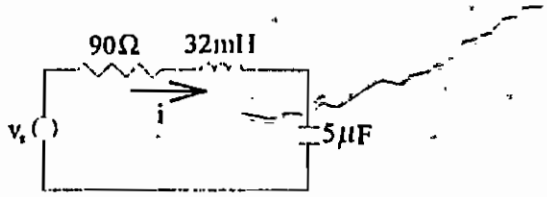

Fig.2

3. (10%) An op amp having a low-frequency gain of 1000 and a single-pole rolloff at 10000 rad/s is connected in a negative-feedback network having a transmission k and a two-pole rolloff at 10000 rad/s. Find the value of k above which the closed-loop amplifier becomes unstable.

4.(30%) A two-stage CMOS amplifier resembling that in Fig.3 is found to have a slew rate of 5V/μs and an unit-gain frequency f_t=2MHz. (a) If the first-stage bias current (2I) is 50μA, what value of C_c must be used? (b) If devices with 1-V threshold are used, what gate-to-source bias voltage is used in the input stage? (c) For a process for which $\mu_n C_{OX}$=20μA/V², what W/L ratio applies for the input-stage devices?

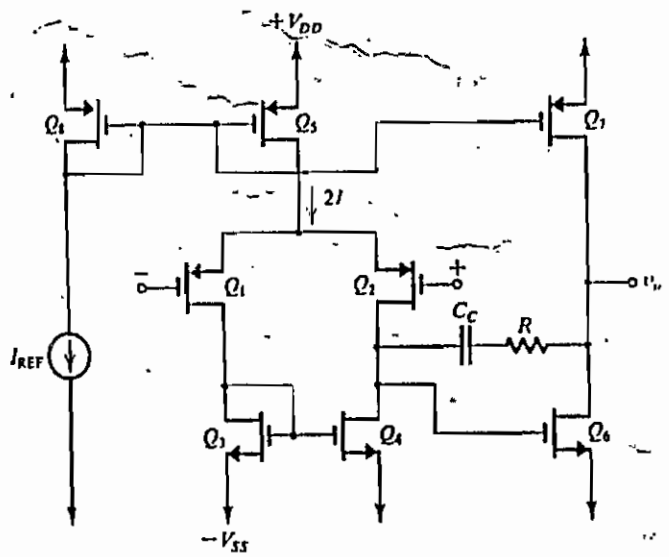

Fig. 3

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所別：電子與資訊工程技術研究所
科目：微分方程

1. Solve the following differential equations (20%)

a. $y^2 \frac{dx}{dy} + xy = x^3$. (10%)

b. $y''(x) + 4\,y(x) = \tan(2x)$, $\forall\, x \in (-\pi/4\ \pi/4)$. (10%)

2. Solve the system (10%)

$\dot{x}_1(t) = 3\ x_1(t) + 2\ \dot{x}_2(t)$

$\dot{x}_2(t) = -3\ x_1(t) - 4\ \dot{x}_2(t) + 4\ e^x$

3. Solve the boundary value problem. (10%)

$\frac{\partial y}{\partial t} = a^2 \frac{\partial^2 y}{\partial x^2}$, for $0 < x < 1$; $t > 0$

$y(0, t) = T_1$, $y(1, t) = T_2$, for $t > 0$,

$y(x, 0) = f(x)$, for $0 < x < 1$.

4. Show that the general solution of

$y''(x) + Ay'(x) + By(x) = 0$

can always be written in the form

$y(x) = [c_1\cos(px) + c_2\sin(px)]\ e^{qx}$

for appropriate choices of p and q, assuming that $A^2 - 4B < 0$. (10%)

5. Solve the following ordinary differential equation. (10%)

$(2x + y^4)y' - y = 0$

6. Find the the series solution by the Frobenius method. (10%)

$(2x^2)y'' + xy' - 3y = 0$

7. What kind of curve is the path in the phase plane? (10%)

$y'' + (y')^2 = 0$

8. Solve the following partial differential equations. (20%)

a. $u_x = 2xyu$. (10%)

b. $u_{xx} = 0$, $u_{yy} = 0$. (10%)

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所別：電子與資訊工程技術研究所
科目：半導體元件

Describe briefly the physical meaning of the following topics:
(a) Early effect (5%) (b) intraband transition (5%)
(c) electron affinity (5%)

A sample of Si (1cm × 1cm × 0.2cm) is measured by the Hall measurement. The measured results are shown in Fig.1 with a magnetic flux density $B = 10^{-4}$ Wb/cm^2. Calculate ① hole and electron concentrations (8%)
② mobility of the majority carrier (7%)

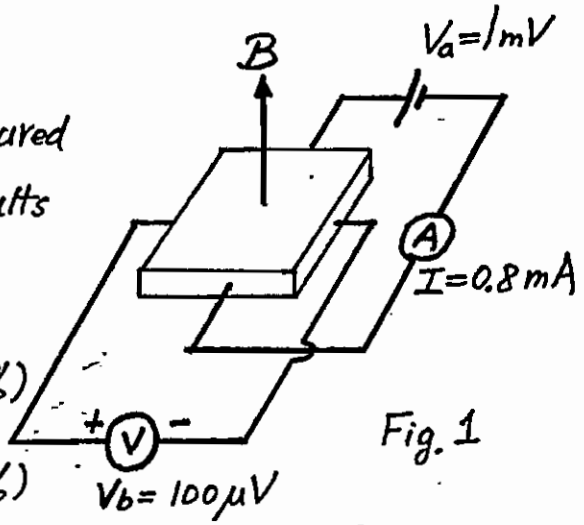

Fig. 1

For a Si diode, as shown in Fig.2, calculate
① the built-in voltage at T=300°K (5%)
② the maximum value of the electric field in the depletion region (5%).
③ the width of the depletion region W (5%)

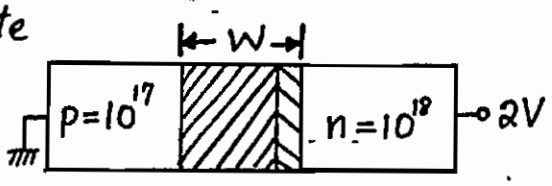

Fig. 2

For an ideal $n^+(10^{19})$-$p(10^{17})$-$n^-(10^{15})$ transistors, find the emitter efficiency and DC current gain. The device parameters are shown in Fig.3. (Note that the generation-recombination currents in the depletion regions are neglected.)

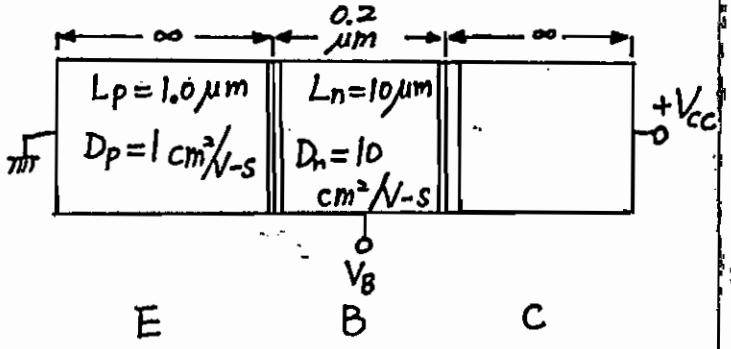

Fig.3

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科目：半導體元件

Sketch the energy band diagrams with various biases to describe the I-V characteristics of a tunneling diode.

Figure 4 shows the measured results of C^{-2} vs. bias for an one-side abrupt Silicon p-n^+ junction. Estimate the doped concentration in the p-side; if n^+-side doping is known as $10^{19}\,cm^{-3}$.

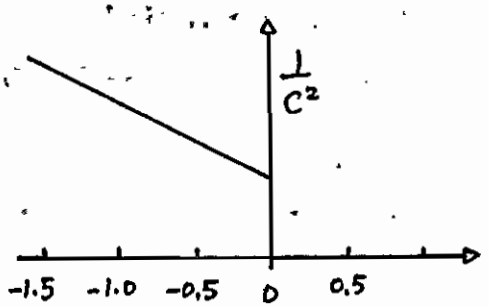

Fig.4

Sketch the device cross sections, output $I_D - V_D$ characteristics and transfer $I_D - V_G$ characteristics to describe n-channel depletion MOSFET and p-channel enhancement MOSFET, respectively.

Si : $E_g = 1.1\,eV$; $n_i^2 = 2.5 \times 10^{20}\,cm^{-6}$ (300°K)

$k = 1.38 \times 10^{-23}\,J/K$ (Boltzmann Constant)

$q = 1.6 \times 10^{-19}\,C$

國立雲林技術學院
八十四學年度研究所碩士班入學考試試題

所別：電機工程技術研究所
電子與資訊工程技術研究所
科目：電子學

1. (a) Explain how to classify power amplifiers of class A, class B, class AB, and class C? (8 %)

   (b) Give an example to illustrate the application of Miller's Theorem? (7 %)

2. (a) Consider the circuit shown in Figure 1(a), in which the devices are assumed to have $V_t = 1$ V, $K = 100\ \mu A/V^2$, and $V_A = 10$ V. If $I_{REF} = 100\ \mu$A and $V_{SS} = 0$ V, then what value of I_o will result? (10 %)

   (b) If the circuit in Figure 1(a) is modified to that in Figure 1(b), what value of I_o results? (5 %)

3. For each of the circuits shown in Figure 2:

   (a) Determine the value of feedback ratio β. (5 %)

   (b) Assume that the loop gain $A\beta$ approaches infinity. What is the gain of the amplifier? What values do the input and the output resistances approach (0 or infinity)? (15 %)

4. Figure 3 shows a circuit suitable for op amp applications. For all transistor $\beta = 100$, $V_{BE} = 0.7$ V, and $r_0 = \infty$.

   (a) For inputs grounded and output held at 0 V (by negative feedback) find the emitter currents of all transistors. (5 %)

   (b) Calculate the gain of the amplifier with a load of 10 kΩ. (5 %)

   (c) With load as in (b) calculate the value of the capacitor C required for a 3-dB frequency of 1 kHz. (5 %)

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科目：電子學

5. Consider the bandpass circuit shown in Figure 4. Let $C_1 = C_2 = C$, $R_3 = R$, $R_4 = R/4Q^2$, $CR = 2Q/\omega_0$, and $\alpha = 1$. Disconnect the positive input terminal of the op amp from ground and apply V_i through a voltage divider R_1, R_2 to the positive input terminal. Analyze the circuit to find its transfer function V_o/V_i. Find the voltage-divider ratio $R_2/(R_1 + R_2)$ so that the circuit realizes (a) an all-pass function and (b) a notch function. Assume the op amp to be ideal. (15 %)

6. An inverter that can be characterized by Figure 5 has $V^+ = 5$ V, $R_L = 1$ kΩ, and $R_{on} = 100$ Ω. It is loaded by a similar inverter whose switching threshold is at 2 V, by means of a connection whose capacitance to ground is 50 pF. If both switches exhibit a pure delay of 10 ns from the moment their input signal threshold is crossed, how long does it take for an input step to open the switch of the second inverter? to close it? (20 %)

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科目：電子學

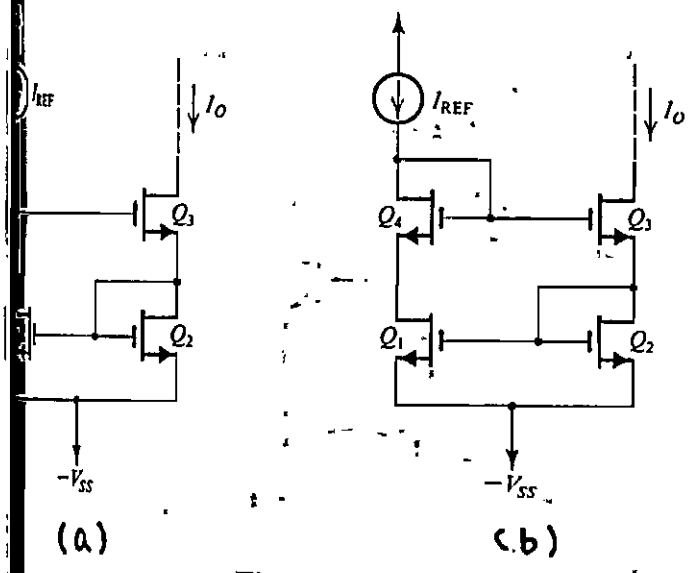

Figure 1

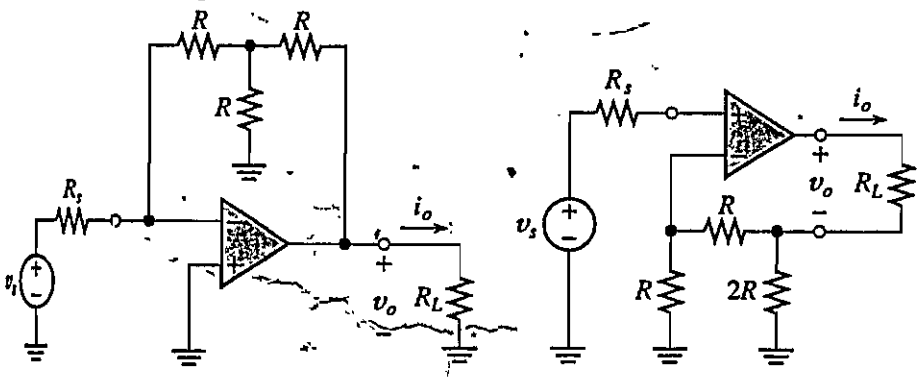

Figure 2

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科目：電子學

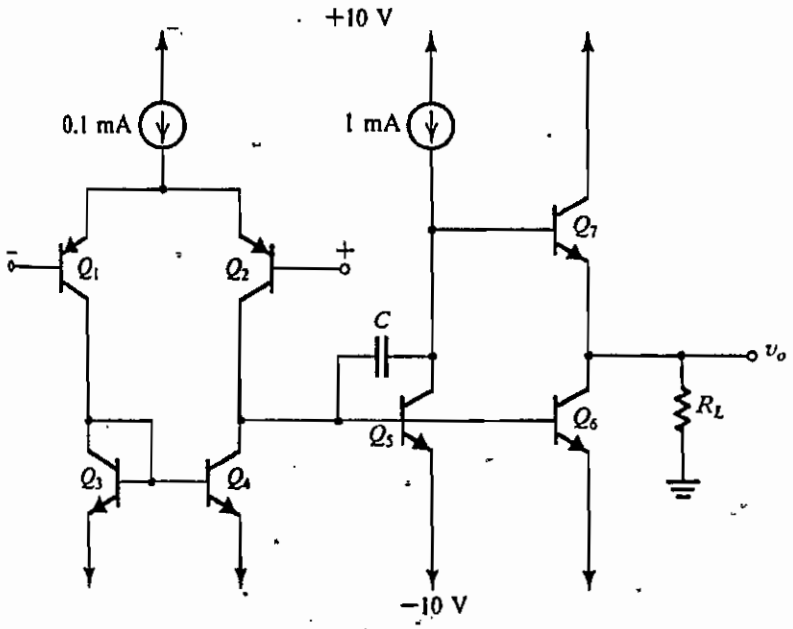

Figure 3

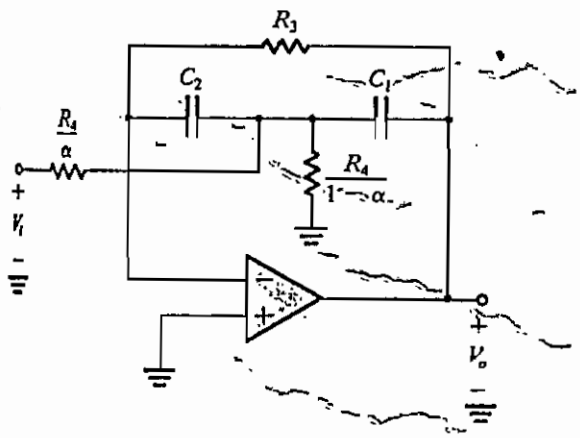

Figure 4

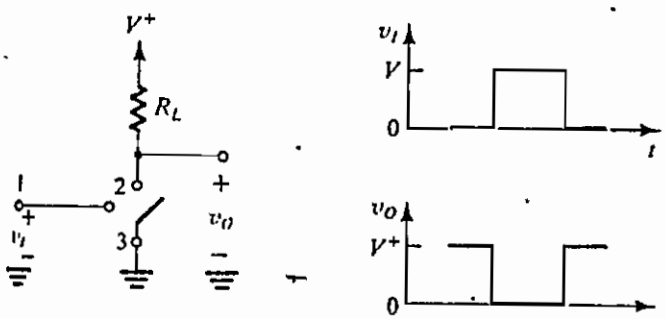

Figure 5