國立雲林技術學院 所別：機械工程技術研究所 電子與資訊工程技術研究所 科目：電子電路
八十三學年度研究所碩士班入學考試試題

注意：1.本試題共 5 題，共 100 分，須標明題號並依序寫在答案卷上，否則不予計分。
2.書寫答案時，由第一頁起橫向左至右依寫，不得倒反。

1. (a) Find the Thévenin equivalent with respect to the terminals a, b for the circuit in Figure 1. (14%)
(b) If an adjustable load R_L is connected to the terminals a and b, find the maximum power transfered to R_L. (6%)

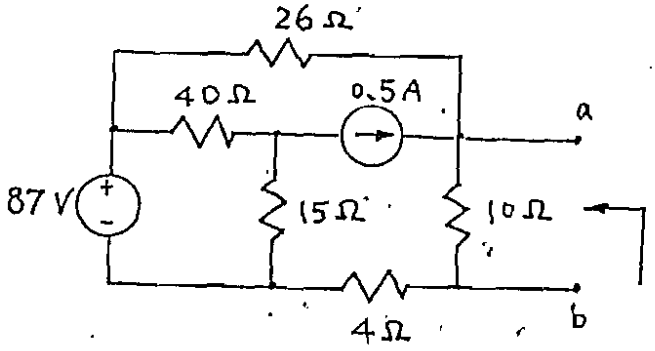

Figure 1

2. In Figure 2, switch 1 has been closed and switch 2 has been opened for a long time. At t=0, switch 1 is opened. One hundred milliseconds later switch 2 is closed. Find
(a) $v_c(t)$ for $0 \le t \le 0.1$s. (10%)
(b) $v_c(t)$ for $0.1s \le t$. (10%)

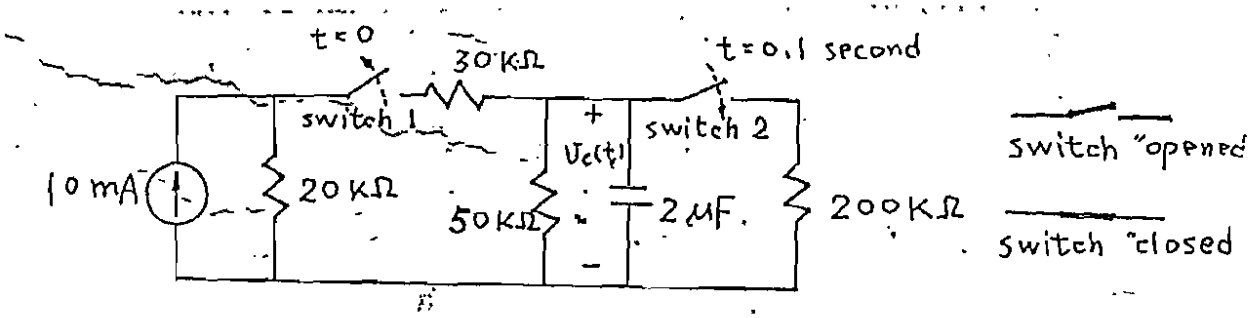

Figure 2

國立雲林技術學院 所別：機械工程技術研究所 電子與資訊工程技術研究所 科目：電子電路
八十三學年度研究所碩士班入學考試試題

3. A bipolar transistor is biased at collector current $I_C = 0.5mA$ and common-emitter forward short-circuit current gain $\beta_0 = 150$
   (a) Determine transconductance g_m at room temperature. (6%)
   (b) The input resistance $h_{ie} = 7.6K\Omega$. Find base-spreading resistance r_b. (6%)
   (c) A load resistance $R_C = 2K\Omega$ is used and the transistor is driven from a 300 Ω voltage source. Estimate the transfer voltage gain. (8%)

4. (a) Draw the low-frequency small-signal model in Figure 3. (10%)
   (b) Derive an expression for the signal component of v_o produced by the signal input v_i. (10%)

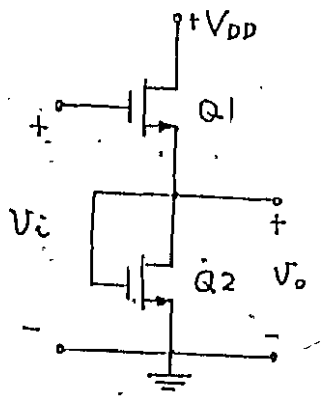

Figure 3

5. The differential- and common-mode gains of a differential amplifier can be approximated as

$$A_{DM} = \frac{-20000}{1 + s/2\pi\times10^6} \text{ and } A_{CM} = \frac{-0.5}{1+s/2\pi\times10^8}$$

   (a) Sketch the asymptotic Bode diagram of the common-mode rejection ratio CMRR. (10%)
   (b) At what frequency is the CMRR one-half its low-frequency value? (10%)

國立雲林技術學院 八十三學年度研究所碩士班入學考試試題 所別：電子與資訊工程技術研究所 電機工程技術研究所 科目：電子學

1. For the circuit of Figure 1, find the voltage gain V_o/V_s, the input resistance R'_{if}, and the output resistance R'_{of}. The op amp has open loop gain $\mu = 10^4$ V/V, $R_{id} = 100$ $K\Omega$, $R_{icm} = \infty$, and $r_o = 1$ $K\Omega$. (12 %)

2. Plot the transfer characteristic $V_o - V_i$ of the circuit in Figure 2. (8 %)

3. Find the logic function implemented by the circuit shown in Figure 3. (6 %)

4. The op-amp system of Figure 4 has a gain function that is

$$G(s) = \frac{10^3 * K}{(1 + s/10^4)^2}$$

$R = 1$ $K\Omega$ and $C = 0.1$ μF.

(a) Determine the closed-loop transfer function $V_o(s)/V_i(s)$. (7 %)

(b) Find the value of k above which the closed-loop system becomes unstable. (5 %)

5. Consider an NMOS invert with enhancement load having $V_{to} = 1$ V, $(W/L)_1 = 4$, $(W/L)_2 = 1/4$, $\mu_n C_{OX} = 20$ $\mu A/V^2$, $2\phi_f = 0.6$ V, $\gamma = 0.5$ $V^{1/2}$, and $V_{DD} = 5$ V.

(a) Neglecting the body effect, find NM_H, and NM_L. (7 %)

(b) Taking the body effect into account, find the modified values of V_{OH} and NM_H. (5 %)

6. Write the transfer function of a second-order notch filter as shown in Figure 5 for which the dc gain is unity, the pole frequency is 10 rad/s, the pole Q is 0.5, and the transmission is zero at 100 rad/s. (10 %)

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7. A FET switch is connected with two load resistors as shown in Figure 6. The intent is to provide somewhat complementary signals at X and Y; that is, when one rises, the other falls. For the FET, $I_{DSS} = 10$ mA and $V_P = -2$V. For the diode, when conducting, $V_D = 0.7$V. When the diode is cut off, what are the voltages at X and Y? What voltage is required at A to ensure that the diode is barely cut off (diode voltage is zero)? What voltage on A is required to cause the JFET to cut off? What voltages on X and Y result? (15 %)

8. In the circuit of Figure 7 all devices are matched. Find the value of V_O. (10 %)

9. Write the transfer function for an amplifier having a gain of -100 at midband and a low-frequency response characterized by zeros at 1 and 10 rad/s (on the negative real axis) and poles at 5 and 100 rad/s. What is the dc gain of this amplifier? What is its 3-dB frequency? (15 %)

國立雲林技術學院 八十三學年度研究所碩士班入學考試試題

所別：電子與資訊工程技術研究所 電機工程技術研究所

科目：電子學

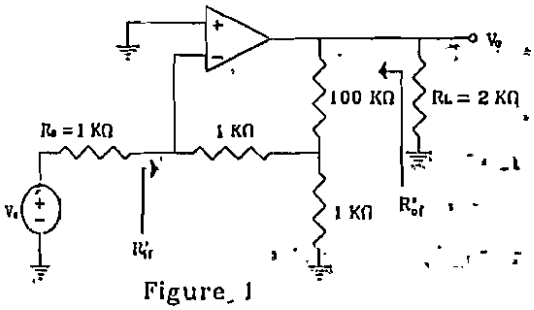


Figure 1

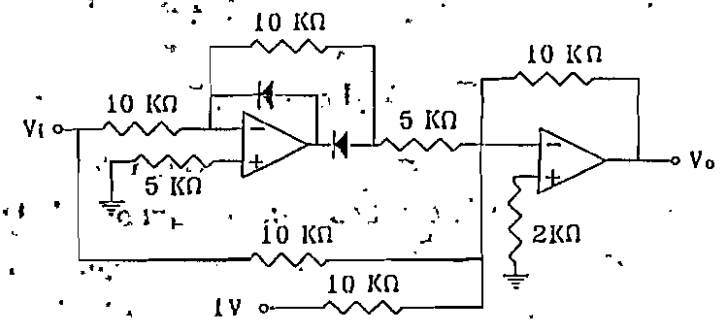


Figure 2

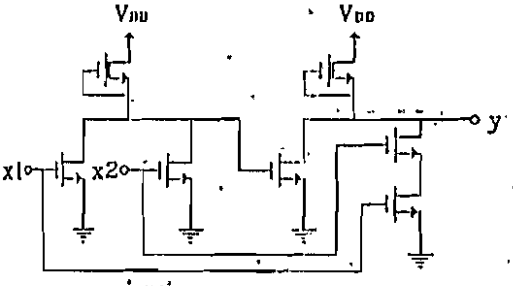


Figure 3

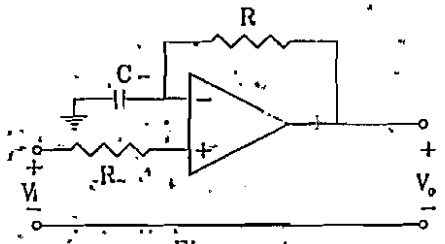
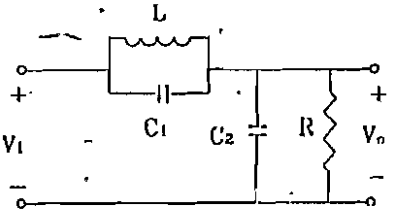


Figure 4



$C_1 + C_2 = C$

Notch: $\omega_n = \frac{1}{\sqrt{LC}}$

Figure 5

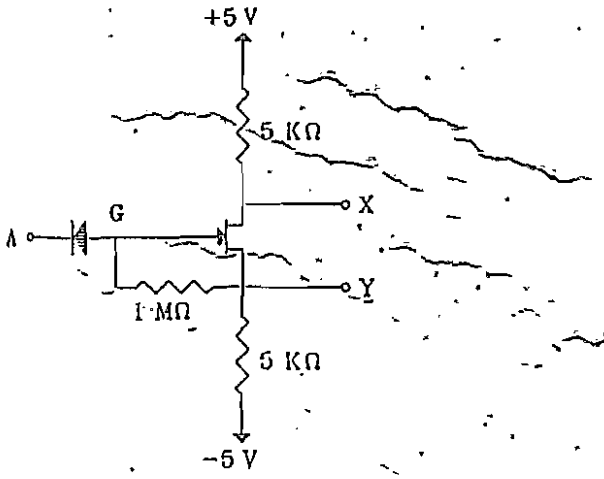


Figure 6

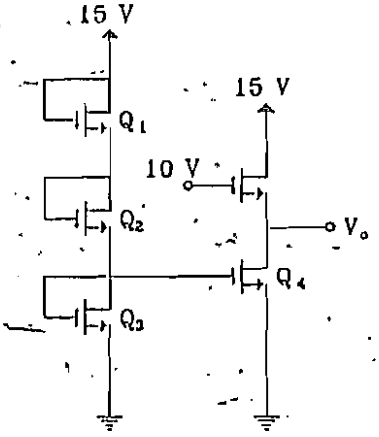


Figure 7

國立雲林技術學院 八十三學年度研究所碩士班入學考試試題 所別 電子與資訊工程技術研究所 科目：工程數學

注意：本試卷共 6 題，共100分；須標明題號，否則不予計分。

(15%) 1. Let $T: \mathbb{R}^2 \longrightarrow \mathbb{R}^3$ be a linear transformation satisfying $T(5,-1) = (1,1,1)$ and $T(-1,5) = (-1,-1,-1)$.

(a) Find the general expression for $T(x_1,x_2)$. (8%)

(b) Find the rank and the nullity of T. (7%)

(15%) 2. The trace of an n×n matrix A is the sum of its entries on the main diagonal that is

$$\text{trace}(A) = \sum_{i=1}^{n} a_{ii}$$

(a) Show that the function $\langle \cdot,\cdot \rangle : \mathbb{R}^{n\times n} \times \mathbb{R}^{n\times n} \longrightarrow \mathbb{R}$ defined by

$$\langle A,B \rangle = \text{trace}(AB^T) \qquad (5\%)$$

is an inner product on $\mathbb{R}^{n\times n}$.

(b) Are the vectors $C = \begin{bmatrix} 2 & 1 \\ 0 & 1 \end{bmatrix}$ and $D = \begin{bmatrix} 1 & -2 \\ 2 & 0 \end{bmatrix}$ orthogonal ? (5%)

(c) In part (b), what is $\|C\|$? And what is $\|C-D\|$? (5%)

(20%) 3. Let $P_2(\mathbb{R})$ be the vector space of polynomials of degree less than or equal to 2. Let $T: P_2(\mathbb{R}) \longrightarrow P_2(\mathbb{R})$ be the linear operator defined by

$T(p(x)) = p(x) + xp'(x) + p''(x)$ ('':differentiation)

Let $\beta = \{1, x, x^2\}$ be the standard ordered basis for $P_2(\mathbb{R})$.

(a) Find the standard matrix representation $[T]_\beta$ of T. (5%)

(b) Find an ordered basis γ for $P_2(\mathbb{R})$ such that the matrix representation of T with respect to γ, $[T]_\gamma$, is a diagonal matrix. (5%)

(c) Find an orthonormal basis for $P_2(\mathbb{R})$ if the inner product on $P_2(\mathbb{R})$ is defined, for any $p(x), q(x) \in P_2(\mathbb{R})$, by

$$\langle p,q \rangle = \sum_{i=1}^{3} p(x_i)q(x_i)$$

where $x_1 = -1$, $x_2 = 0$, and $x_3 = 1$. (10%)

國立雲林技術學院 所別 電子與資訊工程技術研究所 科目：工程數學
八十三學年度研究所碩士班入學考試試題

(20%) 4. Solve the following differential equations.

(a) $\frac{dy}{dx} = \frac{6xy - y^2}{3xy - 6x^2}$ (10%)

(b) $x^2 \frac{dy}{dx} + xy = -1/\sqrt{y^3}$. (10%)

(20%) 5. Solve the initial problems

(a) $y'' - 2yy' = 0$, $y(0) = 0$ and $y'(0) = 1$. (10%)

(b) $y'' + 9y = x\cos(2x)$, $y(0) = 0$ and $y'(0) = 1$. (10%)

(10%) 6. Find the currents in the circuit shown in Fig. 1.

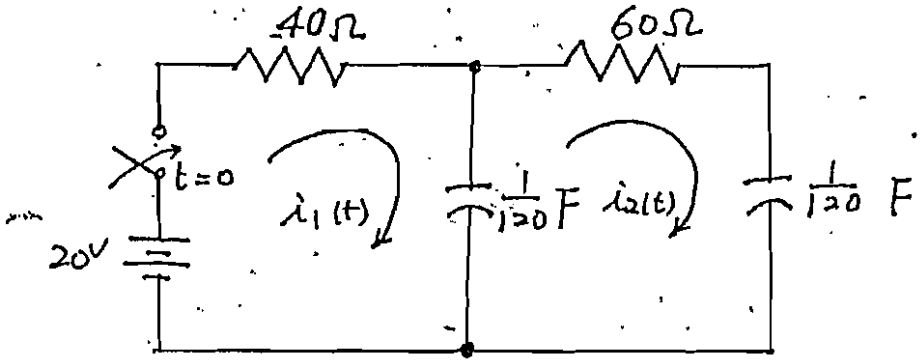


Fig. 1

國立雲林技術學院 八十三學年度研究所碩士班入學考試試題 所別：機械工程技術研究所 電子與資訊工程技術研究所 科目：電子電路

注意：1.本試題共 5 題，共 100 分，須標明題號並依序寫在答案卷上，否則不予計分。
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1. (a) Find the Thévenin equivalent with respect to the terminals a; b for the circuit in Figure 1. (14%)
(b) If an adjustable load R_L is connected to the terminals a and b, find the maximum power transfered to R_L. (6%)

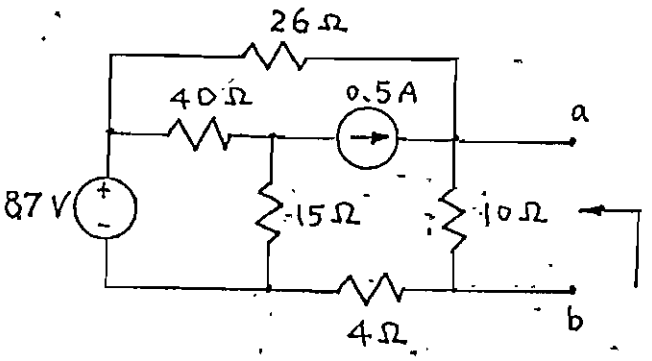

Figure 1

2. In Figure 2, switch 1 has been closed and switch 2 has been opened for a long time. At t=0, switch 1 is opened. One hundred milliseconds later switch 2 is closed. Find
(a) $v_c(t)$ for $0 \le t \le 0.1s$. (10%)
(b) $v_c(t)$ for $0.1s \le t$. (10%)

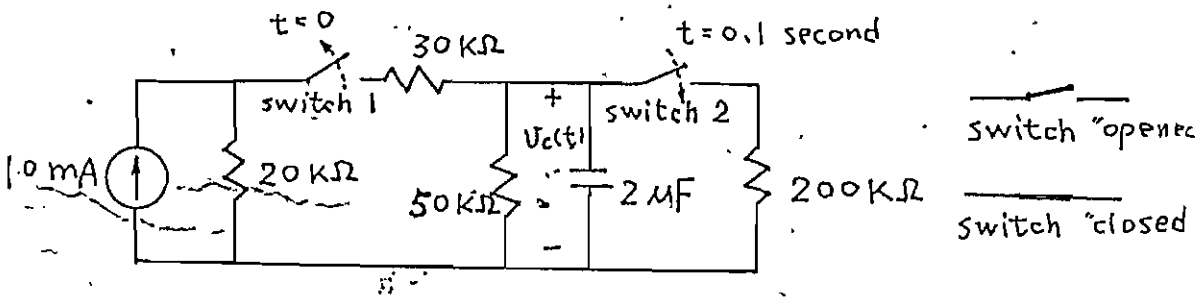

Figure 2

國立雲林技術學院 八十三學年度研究所碩士班入學考試試題 所別：機械工程技術研究所 電子與資訊工程技術研究所 科目：電子電路

3. A bipolar transistor is biased at collector current $I_C = 0.5mA$ and common-emitter forward short-circuit current gain $\beta_0 = 150$
(a) Determine transconductance g_m at room temperature. (6%)
(b) The input resistance $h_{ie} = 7.6K\Omega$. Find base-spreading resistance r_b. (6%)
(c) A load resistance $R_C = 2K\Omega$ is used and the transistor is driven from a 300 Ω voltage source. Estimate the transfer voltage gain. (8%)

4. (a) Draw the low-frequency small-signal model in Figure 3. (10%)
(b) Derive an expression for the signal component of v_o produced by the signal input v_i. (10%)

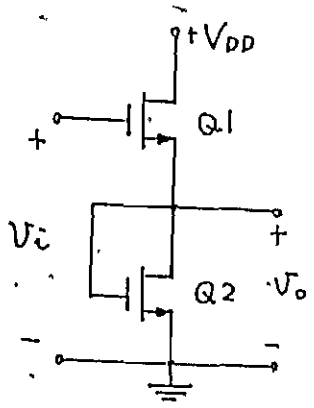

Figure 3

5. The differential- and common-mode gains of a differential amplifier can be approximated as

$$A_{DM} = \frac{-20000}{1 + s/2\pi\times10^6} \text{ and } A_{CM} = \frac{-0.5}{1+s/2\pi\times10^8}$$

(a) Sketch the asymptotic Bode diagram of the common-mode rejection ratio CMRR. (10%)
(b) At what frequency is the CMRR one-half its low-frequency value? (10%)

國立雲林技術學院 八十三學年度研究所碩士班入學考試試題 所別 電子與資訊工程技術研究所 科目：信號與系統

注意：本試卷共 7 題，共100分；須標明題號，否則不予計分。

(15%) 1. Given the system

$$y[n] = \sum_{k=n-2}^{n+4} x[k]$$

where x[n] and y[n] are the system input and output respectively. Determine if the system has the following properties:

(3%) (a) Memoryless
(3%) (b) Time-Invariant
(3%) (c) Linear
(3%) (d) Causal
(3%) (e) Stable

In each case, please justify your answer.

(8%) 2. Given two discrete time signals:
$x1[n] = cos(\frac{3\pi n}{4})$
$x2[n] = sin(\frac{7\pi n}{4})$
Which signal has higher oscillation rate ? please justify your answer.

(12%) 3. x(t) and $X(\omega)$ are fourier transform pair, Prove the following equation:

$$\int_{-\infty}^{\infty} |x(t)|^2 \, dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} |X(\omega)|^2 \, d\omega$$

(Parseval's equation)

(15%) 4. Given an input signal $x[n] = sin(\frac{\pi n}{8}) - 2cos(\frac{\pi n}{4})$ to a LTI system with $h[n] = \frac{sin(\frac{\pi n}{2})}{\pi n}$. What is the output y[n] ?

Hint: Fourier transform of $\frac{sin(Wn)}{\pi n}$ is an ideal lowpass filter with cutoff frequency W.

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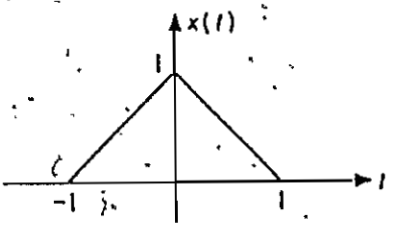
(20%) 5. (a) Find the Fourier transform of the time function shown below. (Hint: Consider $x(t)$ as the convolution of two pulses.) ? (10%)



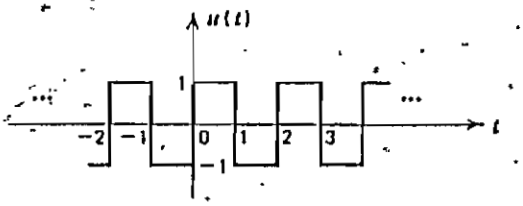
(b) Evaluate the integral

$$\int_{-\infty}^{\infty} \left[\frac{\sin t}{t}\right]^4 dt \qquad (10\%)$$

(15%) 6. The following differential equation is a model for a linear system with input $u(t)$ and output $y(t)$.

$$\frac{dy(t)}{dt} + y(t) = u(t)$$

If the intput $u(t)$ is the square waveform shown, then find the third harmonic in the output.



(25%) 7. Let $x_1(t)$ and $x_2(t)$ be two periodic signals, with a common period of T_0. Define the periodic convolution of $x_1(t)$ and $x_2(t)$ as

$$x_1(t) * x_2(t) = \int_0^{T_0} x_1(\tau)x_2(t-\tau)d\tau = y(t)$$

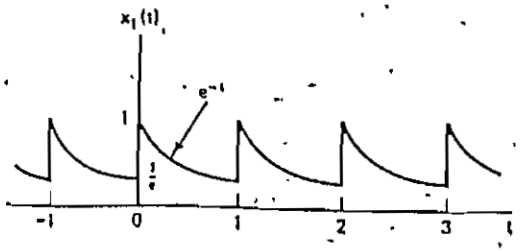
(a) Let

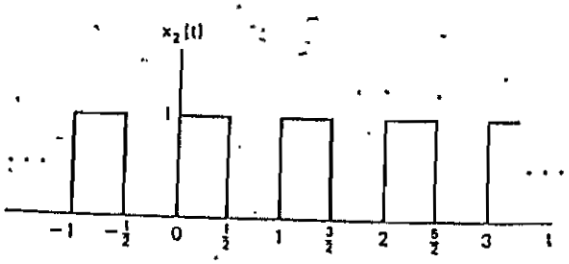
$$y_a(t) = \int_a^{a+T_0} x_1(\tau)x_2(t-\tau)d\tau$$

where a is an arbitrary real number. Show that

$$y(t) = y_a(t) \qquad (7\%)$$

(b) Compute the periodic convolution of the signals shown below, where we take $T_0 = 1$. (8%)





國立雲林技術學院 八十三學年度研究所碩士班入學考試試題 所別 電子與資訊工程技術研究所 科目：數位邏輯

注意：1.本試題共 4 題，共 100 分，須標明題號並依序寫在答案卷上，否則不予計分。
2.書寫答案時，由第一頁起採自左至右橫寫，不得倒反。

1.(25%) (a) The following is a truth table of a 4-input 3-output combinational circuit. Find the simplified Boolean function for outputs A, B, and C as a function of four-inputs D_0, D_1, D_2 and D_3.

inputs				outputs		
D_0	D_1	D_2	D_3	A	B	C
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	0
X	X	1	0	1	1	0
X	X	X	1	1	1	1

note: X don't care

(b) Based on the simplified outputs, design the combinational-circuit with the minimum number of gates (Use only NOT, AND and OR gates).
(c) Describe an application for this circuit.

2.(25%)(a) Why a hazard may occur in the combinational circuit implemented by the Boolean function

$$Y = x_1x_2 + x_2'x_3$$

(b) Design a hazard-free circuit for output Y by adding one more gate. Show the logic diagram.

3.(25%) A sequential circuit has three D flip-flops, A, B, and C, and one input, x. It is described by the following flip-flop input functions:

$$DA = (BC'+B'C)x+(BC+B'C')x'$$

$$DB = A$$

$$DC = B$$

(a) Derive the state table for the circuit.
(b) Draw two state diagram: one for x=0 and the other for x=1.

4.(25%) Design a synchronous BCD counter with JK flip-flops.

乙組

國立雲林技術學院 所別電子與資訊工程技術研究所 科目：計算機概論
八十三學年度研究所碩士班入學考試試題

注意：1. 本試卷共六題，第一、第二、第三、第六題每題十五分，第四、第五題每題二十分，總分爲一百分。
2. 作答時需標明題號，並依序寫在答案卷上，否則不予計分。
3. 書寫答案時，請由第一頁起，採由左自右橫寫。

1. Suppose you must sort a list of six names, and you have already designed an algorithm that will sort a list of four names. Design an algorithm to sort the list of six names by taking advantage of the previously designed algorithm.

2. Insert the keys: *M, T, E, A, Z, G, P,* in the order shown, to build them into an *AVL* tree. Meanwhile, explain what is an *AVL* tree. (Hints: It is a hightly balanced tree.)

3. The Fibonacci numbers are the series of *1, 1, 2, 3, 5, 8, 13,...*. Suppose we wish to compute the *n'th* Fibonacci number. How can we express this problem in a logic language (e.g. Prolog)?

4. State and illustrated at least five language design principles.

5. (a) Find the sum of products form for the following expression.

$$F(A,B,C,D,E) = (\overline{AC} + \overline{D})\,\overline{(B + CE)}$$

(b) The Karnaugh map for a three-input combinational circuit is shown below.

C \ AB	00	01	11	10
0		1		1
1	1		1	

What is the functionality for this circuit? Describe an application for this circuit.

6. Simplify the following Boolean expressions.

(a) $WXY + YZ + X\overline{Y}Z + \overline{X}Y$
(b) $\overline{B}D + \overline{A}B\overline{C} + A\overline{B}C + AB\overline{C}$
(c) $F(A,B,C,D) = \sum(4, 6, 7, 15)$

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注意： 本試題共 10 題，共 100 分，須標明題號，否則不予計分。

1. Prove the Schwarz inequality $|A \cdot B| \leq \|A\| \, \|B\|$, where A and B are two vectors in R^n (10%).

2. Let $L: R^2 \to R^2$ be a linear map. Suppose that
   $L(1,1) = (1,4)$ and $L(2,-1) = (-2,3)$.
   Find $L(3,-1)$ (10%).

3. Find an orthogonal basis for the space of solutions of the linear equation $3x-2y+z=0$ (10%).

4. Compute the ranks of the following matrices (10%):

   a. $\begin{bmatrix} 2 & 1 & 6 & 6 \\ 3 & 1 & 1 & -1 \\ 5 & 2 & 7 & 5 \\ 8 & 3 & 8 & 4 \end{bmatrix}$ b. $\begin{bmatrix} 3 & 1 & 1 & -1 \\ -2 & 4 & 3 & 2 \\ -1 & 9 & 7 & 3 \\ 7 & 4 & 2 & 1 \end{bmatrix}$

5. Find the eigenvalues and a basis for the eigenspaces of the matrix (10%).

$$\begin{bmatrix} 2 & 1 & 0 \\ 0 & 1 & -1 \\ 0 & 2 & 4 \end{bmatrix}$$

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6. Show that $n^4 - 4n^2$ is divisible by 3 for all $n \geq 2$ by induction (10%).

7. A tree is a connected graph without any circuits.
Prove that in a tree, the number of edges is one less than the number of vertices (10%).

8. Forty computers are on sale at a shop. The options available are a CD-ROM, a sound card, and a fax-modem. It is known that among all these computers, 20 have CD-ROM, 12 have sound cards, 10 have fax-modems, and 5 have all three options. Find out at least how many computers do not have any options at all (10%).

9. A high school student wants to prepare for the university entrance exam by working on sample problems in 50 days. He wants to work on at least one problem a day but no more than 90 problems in 50 days. Show that no matter how he schedules the problems, there is a period of consecutive days during which he works on exactly 9 problems (Hint: use the Pigeonhole principle which states that when there are more pigeons than pigeonholes, there must exist one pigeonhole that holds more than one pigeons.) (10%).

10. A village is inhibited by people who either always tell the truth or always tell lies, and who will respond to questions with a "yes" or a "no". A traveller from the city comes to a fork on the road, where one branch leads to a restaurant and the other does not. The traveller wants to go to a restaurant. An inhabitant of the village is at the fork. What sinlge question should the traveller ask him in order to determine which branch to take? (10%)

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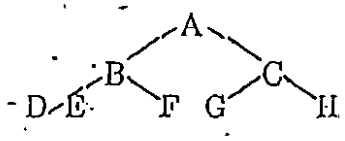
注意： 本試題共 8 題，共 100 分，須標明題號，否則不予計分。

1. List five different addressing modes you know, and explain them (10%).

2. Describe how to process literal operands during Pass1 and Pass2, respectively (15%).

3. Show the overlay definition, using control statements SEGMENT and PARENT, and then calculate each segment's actual address if the starting address is 5000_{16} (15%).

Control section	Length (bytes in hexa. base)
A	2000
B	1500
C	3000
D	1000
E	1800
F	2000
G	800
H	1200



4. Describe the contents of macro processor tables, such as NAMTAB, DEFTAB, and ARGTAB, with an example (10%).

5. Draw the process state–transition diagram and explain the state–transition (10%).

6. State the necessary conditions for the deadlock (10%).

7. In paging memory system with translation–lookaside–buffer (TLB), calculate the average access time (i.e. ? tm—— main–memory access time) if a TLB is 10 times faster than the main memory and the hit ratio is 80% (15%).

8. For a two–address instruction, such as "ADD @x,@y", how many memory references/page faults are required to complete execution of the instruction in the worst case, respectively (Assume that each operation code and operand address is encoded in one word.)? Try to explain each memory reference and page fault, not just giving a number (15%).

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注意： 本試題共四 題，共 100 分，須標明題號，否則不予計分。

(25分)一. Consider the effects of changes to an instruction set.
A load/store machine, Machine A ,has the following instruction mix and clock cycle counts per instruction.

Operation	Frequency	Clock cycle count
ALU ops	43%	1
Loads	21%	2
Stores	12%	2
Branches	24%	2

Machine B is derived by adding a new *register-memory instruction* "ALUnew" to the machine A's instructions. The resulting Machine B changes the instruction mixes by
1. changing the 25% of the original ALU ops to the new ALUnew instructions
2. reducing 25% of the original Loads instructions, and
3. increasing the clock cycle count for Branches by 1.

Assume that the instruction counts for Machine A is 100, and Clock cycle time is a constant.
a. What are the Cycle per Instruction (CPI's) for machines A and B? (13分)
b. What are the CPU times for machines A and B? (12分)

(25分)二. Explain how to use "forwarding (also called bypassing, or short-circuit)" and "pipeline stall (also called bubble)" to resolve pipelining data hazards.
You can use the five-stage instruction cycles IF, ID, EX, MEM, WB. to explain your ideas graphically.
Use the following example code segment to explain the method of "forwarding":

```
ADD   R1, R2, R3   ;add R2 and R3, then store the result into R1.
SUB   R4, R1, R5   ;subtract R5 from R1, store the result into R4.
AND   R6, R1, R7   ;logical AND R1 and R7, store the result into R6.
```

Use the following example code segment to explain the method of "pipeline stall":

```
LW    R1, 32(R6)   ;load a word at location R6+32 into R1
ADD   R4, R1, R7   ;R4 = R1+R7
SUB   R5, R1, R8   ;R5 = R1-R8
```

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(14分)三. a) Consider a system with 28 bits addressing, a 16-KB cache, and the block (line) size is 32 bytes. For the following cases, how many bits are there in the tag? (7分)

- a direct mapped cache
- a fully associative cache
- a 4-way set associative cache

b) Consider the following sequence of addresses. (All are hex numbers) 01AA0050 01AB043 2FE4057 4FFD85F 01AA04E What will be the tag values at the end of the sequence for the direct mapped cache and the 4-way set associative cache in part a). You may assume some initial states and show the initial and final results. (6分)

c) Consider a system that has both a cache and a virtual memory. Assume the virtual address is 32 bits long and mapped into a physical address that is 28 bits long. The cache configuration is 4-way set associative same as the one described in part a). Suppose each page is $P = 2^k$ bytes long. For each memory reference, the virtual address is first translated into a physical address by looking up a page table with $2^{(28-k)}$ entries. The physical address is then used for the cache reference. Suppose that k = 12, work out a scheme that permits you to overlap as much as possible the virtual-memory function and the cache function. Explain your scheme and show the relative timing. (6分)

d) At least 5 bits are required per set to indicate the LRU ordering of the four entries. How would you use just 4 bits to approximate LRU? (6分)

(25分)四. Three devices A, B and C are connected to the bus of a computer. I/O transfers for all three devices use interrupt control. Interrupt nesting for devices A and B is not allowed, but interrupt requests from C are to be accepted while A or B are being serviced. Suggest different ways in which this can be accomplished in each of the following cases

a) The computer has one interrupt-request line and no vectored-interrupt capability. (13分)

b) Two interrupt request lines INTR1 and INTR2 are available, with INTR1 having higher priority. (12分)

Specify when and how interrupts are enabled and disabled in each case.

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1. For the circuit of Figure 1, find the voltage gain V_o/V_s, the input resistance R_{if}, and the output resistance R'_{of}. The op amp has open loop gain $\mu = 10^4\ V/V$, $R_{id} = 100\ K\Omega$, $R_{icm} = \infty$, and $r_o = 1\ K\Omega$. (12 %)

2. Plot the transfer characteristic $V_o - V_i$ of the circuit in Figure 2. (8 %)

3. Find the logic function implemented by the circuit shown in Figure 3. (6 %)

4. The op-amp system of Figure 4 has a gain function that is

$$G(s) = \frac{10^3 * K}{(1 + s/10^4)^2}$$

$R = 1\ K\Omega$ and $C = 0.1\ \mu F$.

(a) Determine the closed-loop transfer function $V_o(s)/V_i(s)$. (7 %)

(b) Find the value of k above which the closed-loop system becomes unstable. (5 %)

5. Consider an NMOS invert with enhancement load having $V_{to} = 1\ V$, $(W/L)_1 = 4$, $(W/L)_2 = 1/4$, $\mu_n C_{OX} = 20\ \mu A/V^2$, $2\phi_f = 0.6\ V$, $\gamma = 0.5\ V^{1/2}$, and $V_{DD} = 5\ V$.

(a) Neglecting the body effect, find NM_H, and NM_L. (7 %)

(b) Taking the body effect into account, find the modified values of V_{OH} and NM_H. (5 %)

6. Write the transfer function of a second-order notch filter as shown in Figure 5 for which the dc gain is unity, the pole frequency is 10 rad/s, the pole Q is 0.5, and the transmission is zero at 100 rad/s. (10 %)

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7. A FET switch is connected with two load resistors as shown in Figure 6. The intent is to provide somewhat complementary signals at X and Y; that is, when one rises, the other falls. For the FET, $I_{DSS} = 10$ mA and $V_P = -2$V. For the diode, when conducting, $V_D = 0.7$V. When the diode is cut off, what are the voltages at X and Y? What voltage is required at A to ensure that the diode is barely cut off (diode voltage is zero)? What voltage on A is required to cause the JFET to cut off? What voltages on X and Y result? (15 %)

8. In the circuit of Figure 7 all devices are matched. Find the value of V_O. (10 %)

9. Write the transfer function for an amplifier having a gain of -100 at midband and a low-frequency response characterized by zeros at 1 and 10 rad/s (on the negative real axis) and poles at 5 and 100 rad/s. What is the dc gain of this amplifier? What is its 3-dB frequency? (15 %) .

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科目：電子學

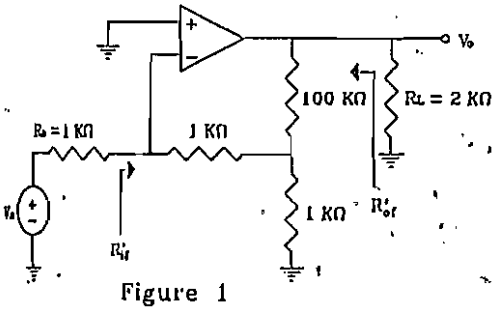


Figure 1

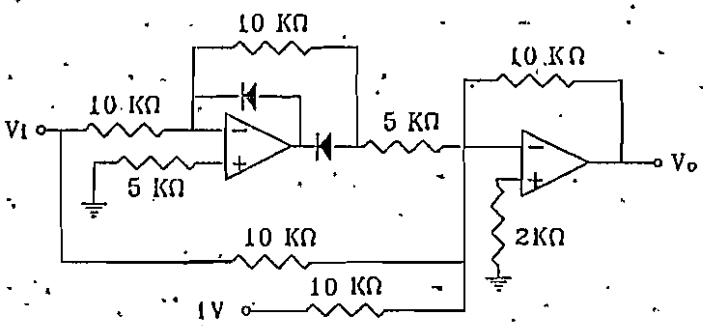


Figure 2

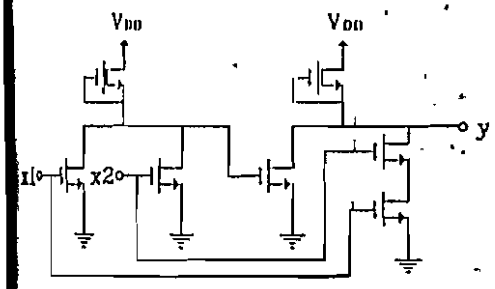


Figure 3

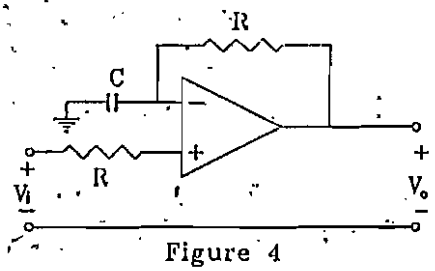
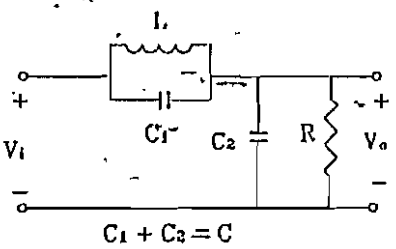


Figure 4



$C_1 + C_2 = C$

Notch: $\omega_n = \frac{1}{\sqrt{LC}}$

Figure 5

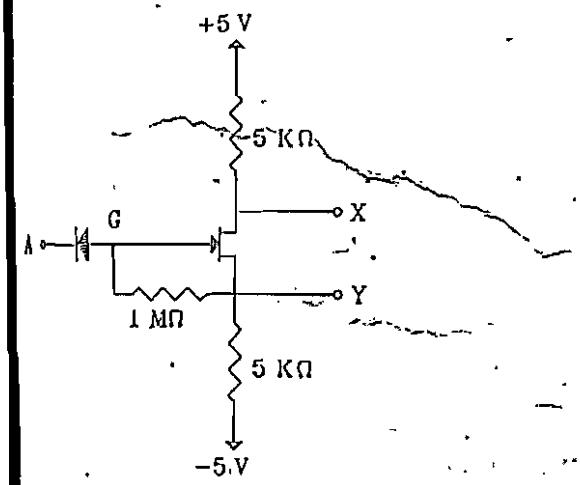


Figure 6

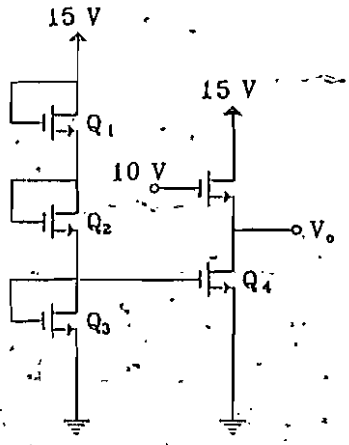


Figure 7

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注意：1、本試題爲問答及計算題，共七題，須標明題號寫在答案卷上，否則不予計分。
2、書寫答案時，由第一頁寫起，不得倒反。

1. From the ambipolar transport equation for excess minority carriers, derive the total current density of the p-n junction in details. (11%)

2. (a) Compare the major differences between the ohmic contacts and rectifying contacts of the metal-semiconductor contacts. (7%)
(b) What are the differences of the Schottky barrier diode and the p-n junction diode. (5%)

3. Sketch the energy band diagrams and the charge distribution in an MOS structure under biasing conditions corresponding to carrier accumulation, depletion, and strong inversion. Use the (a) p-type and (b) n-type substrate, and neglect the effects of surface states and work function difference. [(a)小題：6%; (b)小題：6%]

4.(a) A uniformly doped npn bipolar transistor at T = 300 K is biased in saturation. Starting with the transport equation for minority carriers, show that the excess electron concentration in the base region can be expressed as

$$\delta n_B(x)=n_{B0}\{[\exp(eV_{BE}/KT)-1][1-X/X_B]+[\exp(eV_{BC}/KT)-1][X/X_B]\}$$

for $X_B/L_B \ll 1$,

X_B: neutral base width; L_B: minority carrier diffusion length in the base;

V_{BE}: B-E junction voltage; V_{BC}: B-C junction voltage. (10%)

(b) Derive the minority carrier diffusion current J_n in the base. (5%)

5. A spherical conductor with radius b, as shown in Fig.1, is concentrically surrounded by a dielectric shell with inner radius R_i (> b) and outer radius R_o. The dielectric constant of the shell is ε_r. A total charge Q is uniformly distributed on the surface of sphere. Determine the electric field intensity **E** and the polarization **P** as functions of the radial distance R in the regions: (a) $b \le R \le Ri$; (b) $Ri \le R \le Ro$; and (c) $R \ge Ro$. [(a)小題：5%; (b)小題：5%; (c)小題：5%]

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6. Consider the region enclosed on three sides by grounded conducting planes shown in Fig.2. The end plate on the top surface is insulated from the grounded sides and has a potential $V = V_0\sin(\pi x/a)$, where V_0 is a constant. All planes are assumed to be infinite in extent in the z-direction. Determine the potential distribution within the region. (20%)

7. Referring to Fig.3, a long straight wire of radius a has a circular hole of radius b parallel to the axis of the wire but displaced from the center by a distance c. A current I flows in the wire and is uniformly distributed across the conductor (the shaded region in Fig.3). Find the magnetic flux density B at the center of the hole. (b + c < a) (15%)

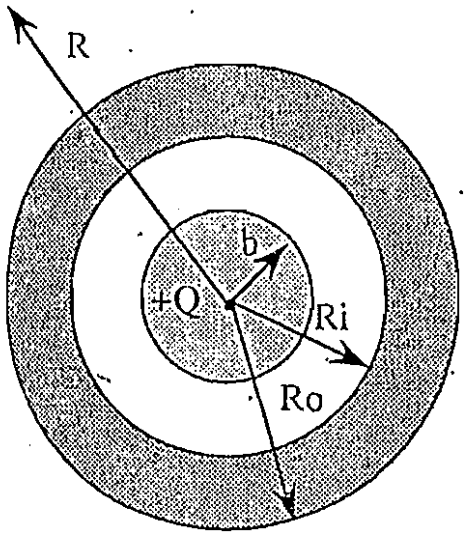

Figure 1

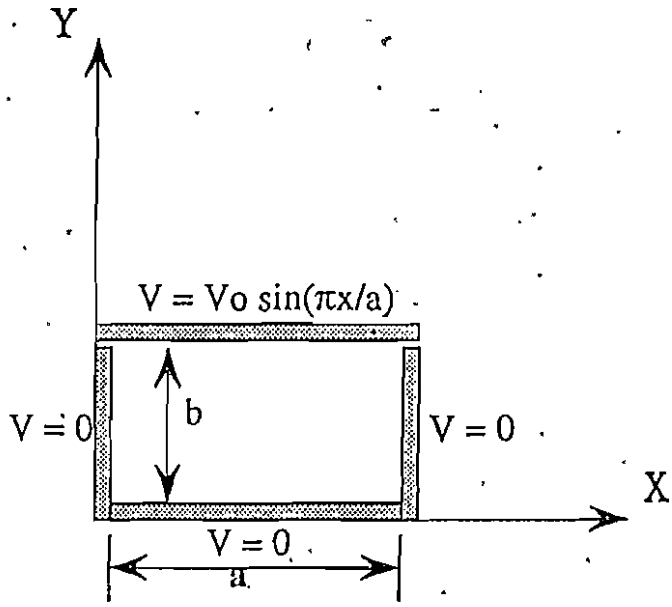

Figure 2

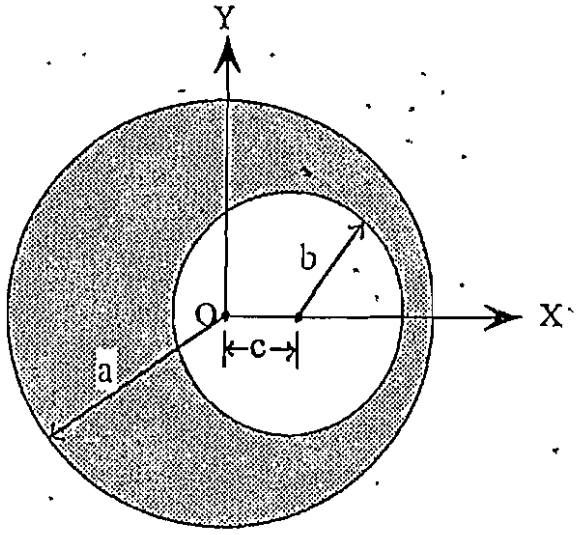

Figure 3

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附錄：第一題至第四題相關之參數或常數：

Appendix A System of Units, Conversion Factors, and General Constants

A.1 Physical constants

Avogadro's number	$N_A = 6.02 \times 10^{+23}$ atoms per gram molecular weight
Boltzmann's constant	$k = 1.38 \times 10^{-23}$ J/K $= 8.62 \times 10^{-5}$ eV/K
Electronic charge (magnitude)	$e = 1.60 \times 10^{-19}$ C
Free electron rest mass	$m_0 = 9.11 \times 10^{-31}$ kg
Permeability of free space	$\mu_0 = 4\pi \times 10^{-7}$ H/m
Permittivity of free space	$\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm $= 8.85 \times 10^{-12}$ F/m
Planck's constant	$h = 6.625 \times 10^{-34}$ J-s $= 4.135 \times 10^{-15}$ eV-s
$\frac{h}{2\pi} =$	$\hbar = 1.054 \times 10^{-34}$ J-s
Proton rest mass	$M = 1.67 \times 10^{-27}$ kg
Speed of light in vacuum	$c = 2.998 \times 10^{10}$ cm/s
Thermal voltage ($T = 300$°K)	$V_t = \frac{kT}{e} = 0.0259$ volt $kT = 0.0259$ eV

A.2 Silicon, gallium arsenide, and germanium properties ($T = 300$°K)

Property	Si	GaAs	Ge
Atoms (cm^{-3})	5.0×10^{22}	4.42×10^{22}	4.42×10^{22}
Atomic weight	28.09	144.63	72.60
Crystal structure	Diamond	Zincblende	Diamond
Density (g/cm^{-3})	2.33	5.32	5.33
Lattice constant (Å)	5.43	5.65	5.65
Melting point (°C)	1415	1238	937
Dielectric constant	11.7	13.1	16.0
Bandgap energy (eV)	1.12	1.42	0.66
Electron affinity, χ, (volts)	4.01	4.07	4.13
Effective density of states in conduction band, N_c, (cm^{-3})	2.8×10^{19}	4.7×10^{17}	1.04×10^{19}
Effective density of states in valence band, N_v, (cm^{-3})	1.04×10^{19}	7.0×10^{18}	6.0×10^{18}
Intrinsic carrier concentration (cm^{-3})	1.5×10^{10}	1.8×10^{6}	2.4×10^{13}

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附錄：第一題至第四題相關之參數或常數：

Appendix B System of Units, Conversion Factors, and General Constants

B.1 *(concluded)*

Property	Si	GaAs	Ge
Mobility (cm^2/V-s)			
Electron, μ_n	1350	8500	3900
Hole, μ_p	480	400	1900
Effective mass, $\left(\frac{m^*}{m_0}\right)$			
Electrons	$m_l^* = 0.98$	0.067	1.64
	$m_t^* = 0.19$		0.082
Holes	$m_{lh}^* = 0.16$	0.082	0.044
	$m_{hh}^* = 0.49$	0.45	0.28
Effective mass (density of states)			
Electrons, $\left(\frac{m_n^*}{m_0}\right)$	1.08	0.067	0.55
Holes, $\left(\frac{m_p^*}{m_0}\right)$	0.56	0.48	0.37

B.2 Other semiconductor parameters

Material	E_g (eV)	a (Å)	ϵ_r	χ	$\bar{n}$
Aluminum arsenide	2.16	5.66	12.0	3.5	2.97
Gallium phosphide	2.26	5.45	10	4.3	3.37
Aluminum phosphide	2.43	5.46	9.8		3.0
Indium phosphide	1.35	5.87	12.1	4.35	3.37

B.3 Properties of SiO_2 and Si_3N_4 ($T = 300°K$)

Property	SiO_2	Si_3N_4
Crystal structure	[Amorphous for most integrated circuit applications]	
Atomic or molecular density (cm^{-3})	2.2×10^{22}	1.48×10^{22}
Density ($g\text{-}cm^{-3}$)	2.2	3.4
Energy gap	≈9 eV	4.7 eV
Dielectric constant	3.9	7.5
Melting point (°C)	≈1700	≈1900

$$D_p \frac{\partial^2(\delta P_n)}{\partial x^2} - \mu_p E \frac{\partial(\delta P_n)}{\partial x} + g' - \frac{\delta P_n}{\tau_{p0}} = \frac{\partial(\delta P_n)}{\partial t}$$

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2.書寫答案時，由第一頁寫起，不得倒反。
3.作答前，務必詳讀每題之提示及說明，不依規定者，不予計分。
4.評分將依據作答內容是否具體、明確、完整等。

一、本大題分為 (a)、(b)、(c)三小題，報考在職生選考甲組者只作 (a)小題（(b)、(c)小題不准作答），選考乙組者只作 (b)小題（(a)、(c)小題不准作答），選考丙組者只作 (c)小題（(a)、(b)小題不准作答）。若違反上述規定者，本大題一律不予計分。（４０分）

(a) 當電路或系統的規格確定後，你可能從頭著手設計或利用現有的電子元件或模組來組合，依你的經驗，請描述實現的策略或方法，設計時考量的重點，預期所需之輔助設備及如何驗証你的設計會符合規格？

(b) 試以I/O，或記憶體系統，或CPU架構，或作業軟體提出一值得研究探討之問題及可能解決之道。請詳述問題之根源，為何值得探討或改進，以及尋求解決方法之可能步驟。

(c) 請試述三種光電元件之基本工作原理、結構、材料之特性與比較、應用範疇以及未來發展趨勢。並請針對三種光電元件及材料之特性分析，提出您曾接觸之檢測技術及方法。

二、請就您從事的專業領域，列舉出二個解決問題的實務經驗範例，並請詳加以說明問題之根源、改善方法、理論依據、技術需求以及改善後之成效。（３０分）

三、請詳述下列問題：（３０分）

(a) 在六年國建計畫中之十大新興產業及八大關鍵性技術中，與本所（電子與資訊工程技術研究所）直接關聯者有那些？

(b) 碩士班研究所階段之讀書研究計畫。

(c) 依您大學教育之背景及工作之經驗，研究所教育應如何加強與產業界之關係，俾使學校之教學與研發能與產業界需求相互配合。