1. Let R_s=1$k\Omega$ in the circuit of Fig. 1, find v_1, v_2, v_0, i_s, i_1, and i_f as function of v_s for (a) $R_f=\infty$ and (b) R_f=40$k\Omega$. (20%)

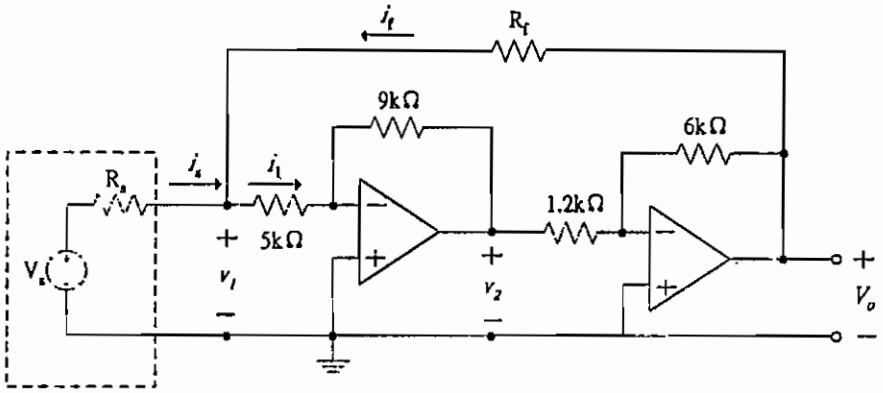

Fig. 1

2. In the RC circuit shown in Fig. 2, the switch is closed on position 1 at t=0 and then moved to 2 after the passage of one time constant. Obtain the current transient for (a) 0 <t <τ (b) t >τ (20%)

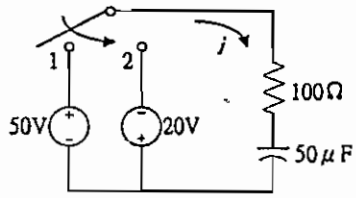

Fig. 2

3. In the network shown in Fig. 3, the two equal capacitances C and the shunting resistance R are adjusted until the detector current I_D is zero. Assuming a source angular frequency ω, determine the values of R_x and L_x. (10%)

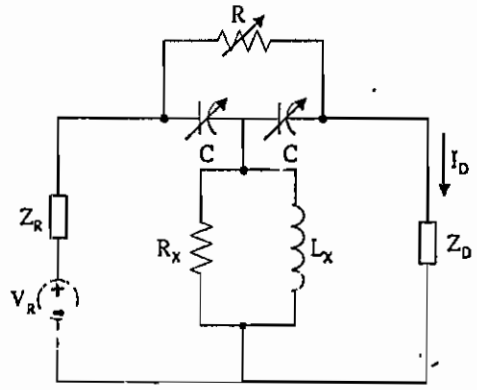

Fig. 3

國立雲林科技大學
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系所：電機系
科目：電路學

4. A three-phase, three-wire, balanced, Δ-connected load yields wattmeter readings of 1154 W and 577W. Obtain the load impedance, if the line voltage is 141.4V. (10%)

5. For the RLC series circuit shown in Fig. 4, (a) derive the half power frequencies ω_l and ω_h (b) derive the quality factor Q. (20%)

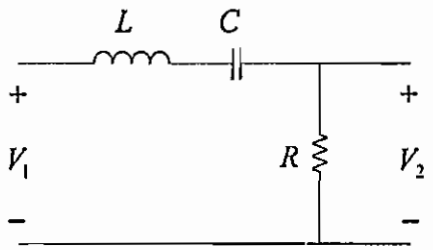

Fig. 4

6. Considering the autotransformer shown in Fig. 5 ideal, obtain the currents $\mathbf{I}_1$, $\mathbf{I}_{cb}$, and $\mathbf{I}_{dc}$. (20%)

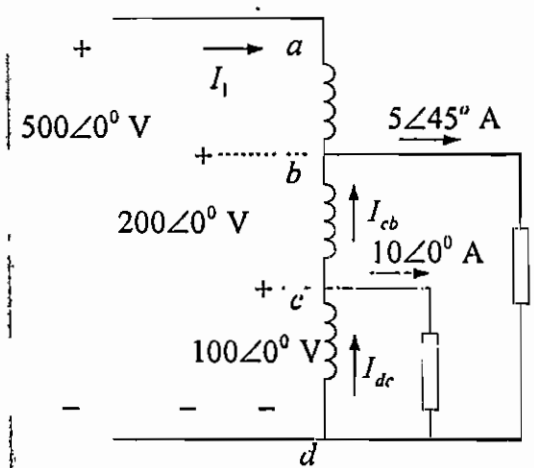

Fig. 5

國立雲林科技大學
98學年度碩士班入學招生考試試題

系所：電機系
科目：電力系統

1. The real power delivered by a source to two impedances, Z_1=3+j5 Ω and Z_2=10 Ω, connected in parallel, is 2000 W. Determine (a) the real power absorbed by each of the impedances (10%), and (b) the source current (10%).

2. For a conceptual single-phase, phase-shifting transformer, the primary voltage leads the secondary voltage by 30° . A load connected to the secondary winding absorbs 50 kVA at 0.9 power factor leading and at a voltage $E_2 = 277\angle 0°$ volts. Determine (a) the primary voltage (6%), (b) the primary and secondary currents (8%), (c) the load impedance referred to the primary winding (8%), and (d) the complex power supplied to the primary winding (8%).

3. A 30-km, 34.5-kV, 60-Hz three-phase line has a positive-sequence series impedance $z = 0.19 + j0.34\,\Omega/\text{km}$. The load at the receiving end absorbs 10 MVA at 33 kV. Assuming a short line, calculate: (a) the *ABCD* parameters (10%), (b) the sending-end voltage for a load power factor of 0.9 lagging (10%).

4. Given the open-delta PT connection shown in Figure 1, both PTs having a voltage rating of 240 kV : 120 V, the voltages are specified as $V_{AB} = 230\angle 0°$, $V_{BC} = 230\angle -120°$, and $V_{CA} = 230\angle 120°$ kV. Determine V_{ab}, V_{bc}, and V_{ca} for the following cases: (a) The dots are shown in Figure 1 (10%). (b) The dot near c is moved to b in Figure 1 (10%).

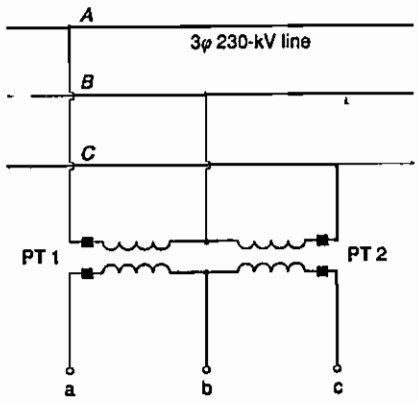

Figure 1

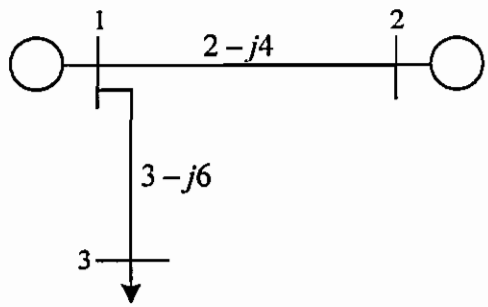

Figure 2

5. Consider the simplified electric power system shown in Figure 2. The values marked are admittances. Compute the elements of the bus admittance matrix Y_{bus} (10%).

國立雲林科技大學
98學年度碩士班入學招生考試試題

系所：電機系
科目：工程數學

本試題共 7 題，共計 100 分，請依題號作答並將答案寫在答案卷上，違者不予計分。

1. Solve the general solution of differential equations: (本題共 25 分)

(1) $\frac{dy}{dx}=2x+1$ (5 分)

(2) $\frac{dy}{dx}=-\frac{y^2}{1+3xy}$ (10 分)

(3) $[(x-2)^3D^3+(x-2)^2D^2+4(x-2)D]y=3(x-2)^2$

[Note: $D^n y=y^{(n)}=\frac{d^n}{dx^n}y$] (10 分)

2. Let $A=\begin{bmatrix}1&0&-1\\1&2&1\\2&2&3\end{bmatrix}$, (本題共 25 分)

(1) find the eigenvalues and eigenvectors of the matrix A, (5 分)

(2) find P and P^{-1}, then diagonalize the matrix A by $D=P^{-1}AP$, (5 分)

(3) $\left[A^3-6A^2+11A-7I\right]^3=?$ (5 分)

(4) If $X(t)=\Omega(t)C$ is the general solution of the system $X'=AX$, find the fundamental matrix $\Omega(t)=?$ (10 分)

3. Use the Laplace transform to solve the integral equation:

$y(t)=3+\int_0^t y(\alpha)\cos[2(t-\alpha)]d\alpha$ (本題共 10 分)

4. Use the Laplace transform to solve the initial value problem:

$\begin{cases}3x'-y=4t\\x'+y'-y=0\end{cases}$, $x(0)=y(0)=0$. (本題共 10 分)

5. Find the inverse Laplace transform of

$G(s)=e^{-4s}\ln\left\{\left[(s-2)^2+3^2)\right]^2/(s^2-4^2)^3\right\}$ (本題共 10 分)

6. If $f(x)=x^2$ for $0\le x\le 2$, find its either (a) Fourier cosine series or (b) Fourier sine series (In other words, please work our only (a) or only (b), and your should clearly indicate your choice). (本題共 10 分)

7. If the Fourier transform of $f(t)=e^{-at}u(t)$ is $F(\omega)=\frac{1}{a+j\omega}$, find the inverse Fourier transform of $G(\omega)=\frac{e^{j(2\omega-7)}}{5+j(\omega-3)}$ (本題共 10 分)

國立雲林科技大學
98學年度碩士班入學招生考試試題

系所：電機系
科目：自動控制

1. Consider a electrical network shown in Figure 1. Find a state-space representation (state equation and output equation) if the output is the current through the resistor $i_R(t)$. (15%)

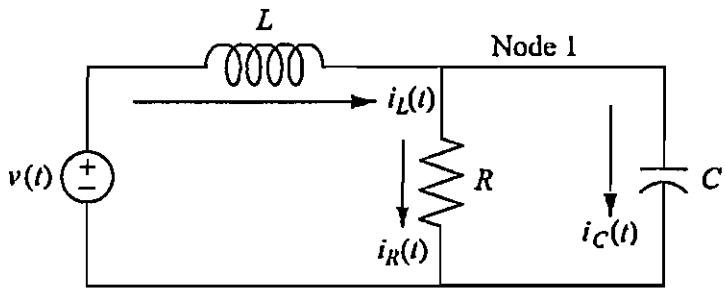

Figure 1

2. Consider a unity feedback control system shown in Figure 2 for the open-loop transfer function $G(s)=\dfrac{k}{(s+10)(s^2+4s+5)}$.

(i) Find the range of k for the system to be stable ? (10%)

(ii) Find the actual location of the closed-loop one negative and two conjugate poles when the system is marginally stable ? (10%)

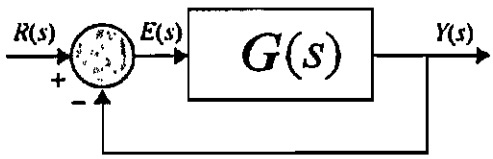

Figure 2

3. Consider a unity feedback system shown in Figure 2 for the open-loop transfer function $G(s)=\dfrac{60(s+1)}{s(s-28)}$.

(i) Find the output response $y(t)$ for the unit step input $(r(t)=1,\ t\geq 0)$. (10%)

(ii) Find the settling time for the output response $y(t)$ to reach and stay within 2% of the final value. (5%)

4. Consider the unity feedback system shown in Figure 3.

(i) Make an *accurate* plot of the root locus. (10%)

(ii) Find the breakaway and break-in points. (5%)

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系所：電機系
科目：自動控制

(iii) Find the range of K to keep the system stable. (5%)

(iv) Find the value of K that yields a stable system with critically damped second-order poles. (5%)

(v) Find the $j\omega$ – axis crossing. (5%)

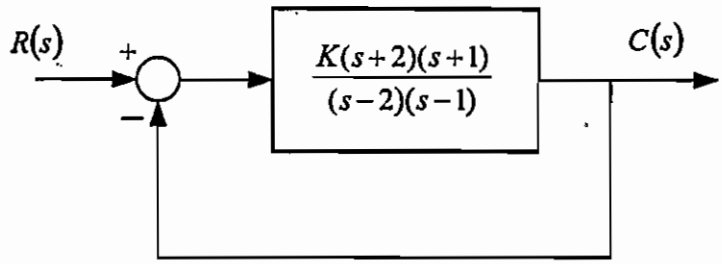


Figure 3

5. Consider the system shown in Figure 4.

(i) Find the range of K for stability by using the Nyquist criterion. (10%)

(ii) Given $K = 0.1$, find the gain margin and phase margin of the system. (10%)

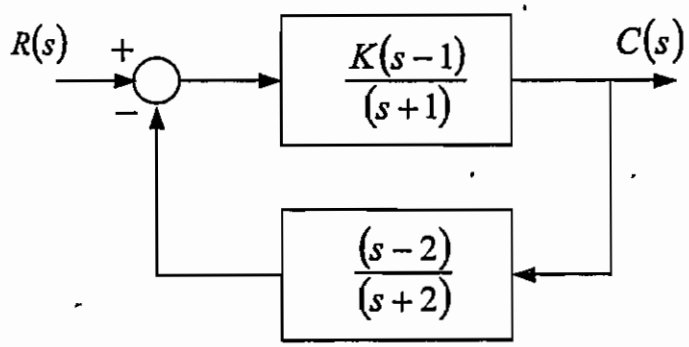


Figure 4

國立雲林科技大學
98學年度碩士班入學招生考試試題

系所：電機系
科目：計算機概論

本試題共十題，每題10分，共計100分，請依題號作答並將答案寫在答案卷上，違者不予計分。

1. 名詞解釋：
   (a) (5%)請說明在作業系統中，行程(Process)與執行緒(Thread)之差異？
   (b) (5%)請說明在韌體設計時，輪詢迴圈(Polling Loop)機制與中斷觸發(Interrupt Driven)機制之差異？

2. 有一個處理器的運作時脈為200 MHz。表一是此處理器在執行特定組合語言指令時所需的Cycle Per Instruction (CPI)。表二是編譯器在解析某個範例程式時所得的組合語言指令結構與數量：
   (a) (5%)請問處理器在執行這個範例程式時所需的CPI？
   (b) (5%)請問處理器在執行這個範例程式時可以實現的 Million Instructions Per Second (MIPS)？

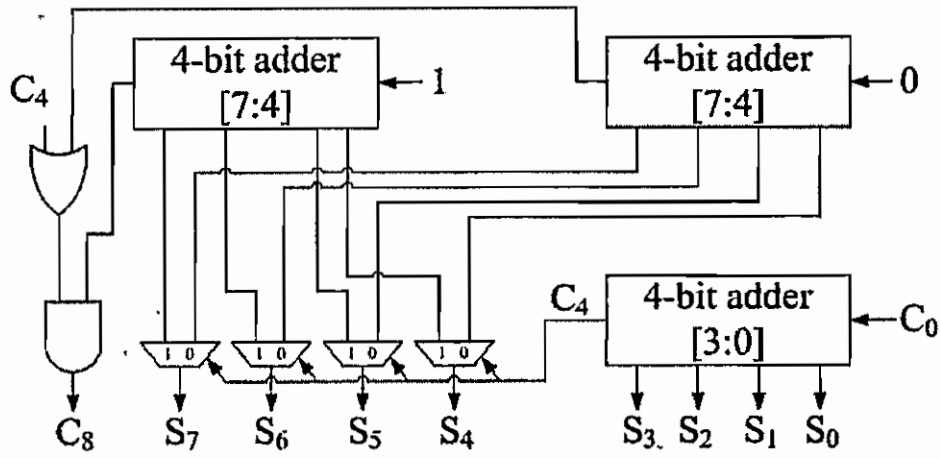
表一

組合語言指令	所需的CPI
A	4
B	2
C	1

表二

組合語言指令	數量
A	5
B	2
C	1

3. 圖一是一個八位元全加法器的架構圖：
   (a) (3%)請問圖一是哪一種架構的全加法器？
   (b) (3%)請問圖一的八位元全加法器的運作原理？
   (c) (4%)請問圖一的八位元全加法器的優點與缺點？



圖一

國立雲林科技大學
98學年度碩士班入學招生考試試題

系所：電機系
科目：計算機概論

4. 有一個處理器可以進行六階(Stage)的管線(Pipeline)加速運算，可是其中第三階的運算需要2個時鐘週期(Clock Cycle)的運算時間，第五階的運算需要3個時鐘週期的運算時間，至於其它階的運算都只需要1個時鐘週期的運算時間：
   (a) (5%)在沒有 Hazard 的理想狀況下，請畫圖說明這個處理器執行4個指令所需要的時鐘週期為何？
   (b) (5%)在沒有 Hazard 的理想狀況下，這個處理器執行 n 個指令所需要的時鐘週期為何？

5. 一般處理器的組合語言指令集(Assembly Instruction Set)，可以分成精簡指令集(RISC)與複雜指令集(CISC)，二大類。請問：
   (a) (5%)為何精簡指令集(RISC)型的處理器比較常被嵌入式系統領域所採用？
   (b) (5%)為何精簡指令集型處理器與複雜指令集型處理器的未來發展都勢必走向多核心(Multicore)的架構？

6. (10%) 試描述或以圖繪的方式說明中斷處理（interrupt handling）的執行步驟。

7. (10%) 試以 shared-memory 方式描述一個能解決 bounded-buffer producer-consumer 問題的方式。(所使用之資料結構請自行設計)

8. (5%) 請說明網路通訊之「線路交換」（circuit switching）及「分封交換」（packet switching）的工作方式。
   (5%) 比較「線路交換」與「分封交換」之不同點。

9. (5%) 何謂網路釣魚（phishing）？
   (5%) 在使用網際網路(Internet)應用服務時，我們常使用 cookie。請說明 cookie 有何用處？

國立雲林科技大學
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系所：電機系
科目：計算機概論

10. (10%) 下列圖二為 Java 程式，請寫出該程式的輸出結果：

```
public class YunTechExam
{   // 主程式
    public static void main(String[] args)
    {  // 變數宣告
       int x, y;
       x = y = 10;
       System.out.println("x++ = "+x+++":x = "+x);
       System.out.println("--y = "+--y+":y = "+y);
    }
}
```

圖二

國立雲林科技大學
98學年度碩士班入學招生考試試題

系所：電機系
科目：資料結構

本試題共十題，共計 100 分，請依題號作答並將答案寫在答案卷上，違者不予計分。

1. 求解下列二個程式的迴圈執行次數：

(a) (5%)

```
for i = 1 to n
    for j = i to n
        for k = j to n
        end of k loop
    end of j loop
end of i loop
```

(b) (5%)

```
for i = 1 to n
    j = i
    while j >= 2 do
        j = j div 5
    end of while loop
end of i loop
```

2. 有一個上三角矩陣，如下所示，而且此矩陣以最少的記憶體空間做儲存：

$$\begin{bmatrix} a(1,1) & a(1,2) & a(1,3) & \cdots & a(1,n) \\ 0 & a(2,2) & a(2,3) & \cdots & a(2,n) \\ 0 & 0 & a(3,3) & \cdots & a(3,n) \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & a(n,n) \end{bmatrix}$$

(a) (5%)假設每個元素所需的儲存空間為 1 Byte，若 $a(1,1)$ 之儲存位址為 B，而且以 Row-Major 方式做儲存，請問任一元素 $a(i,j)$ 的儲存位址為何？

(b) (5%)假設每個元素所需的儲存空間為 1 Byte，若 $a(1,1)$ 之儲存位址為 B，而且以 Column-Major 方式做儲存，請問任一元素 $a(i,j)$ 的儲存位址為何？

3. (10%)堆疊(Stack)記憶體區段在計算機系統中主要有五種重要的應用，分別是處理 Subroutine Call、處理 Recursive Call、將 Infix 數學表示式轉換為 Postfix 數學表示式、二元樹追蹤及 Stack Computer。請解釋堆疊在這五種應用中所扮演的工作角色？

4. (10%)請比較使用鍊結串列(Linked Lists)與陣列(Array)方式來實作堆疊記憶體的優缺點？

	鍊結串列	陣列
優點		
缺點		

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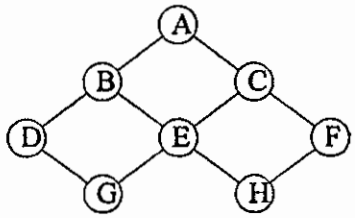
系所：電機系
科目：資料結構

5. (10%) 有一個二元樹(Binary Tree)，如果依照中序(Infix)追蹤法，其順序為EFGBHCDATRS。而如果依照後序(Postfix)追蹤法，其順序為GFEHDCBTSRA。請畫出此二元樹之架構圖，並說明理由？

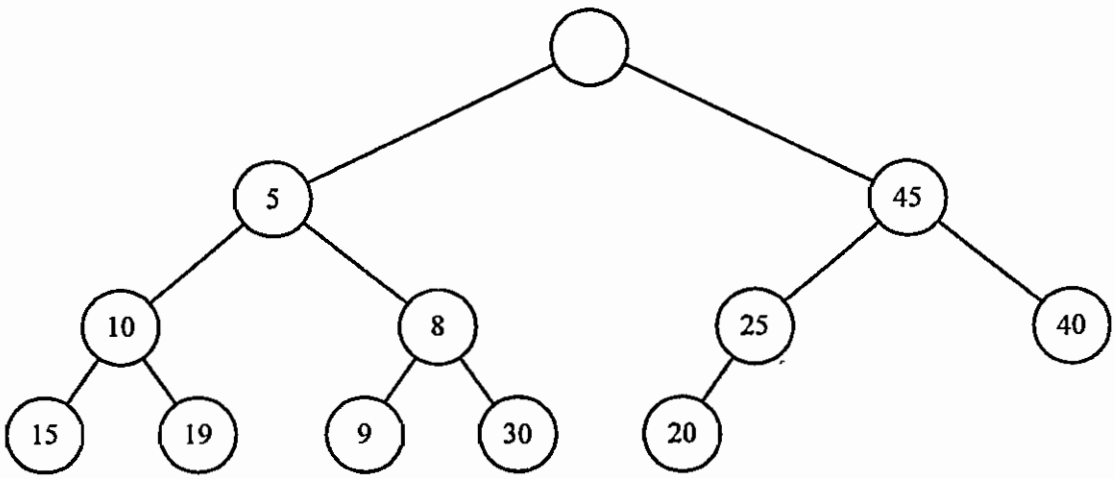
6. (a) (3%) 請說明什麼是圖形走訪(Graph Traversal)，並列舉兩種圖形走訪的應用。
(b) (7%) 考慮如圖一所示的無向圖（Undirected Graph）。請以 pseudo-code 或任何合乎語法的程式語言來描述你所使用的先深後廣搜尋法（Depth-first Search），並依序寫出你所走訪的節點順序（從 A 開始）。



圖一

7. (a) (5%) 試說明內部搜尋（Internal Sorting）和外部搜尋（External Sorting）之差異？
(b) (5%) 能使用費氏搜尋法（Fibonacci Search）的前提為何？

8. 考慮圖二所示之雙堆集樹（deap）。



圖二

國立雲林科技大學
98學年度碩士班入學招生考試試題

系所：電機系
科目：資料結構

(a) (5%) 於圖二插入一個新節點 4，則雙堆集樹變成如何？（請直接繪出結果）
(b) (5%) 自圖二刪除節點 5，則圖二之雙堆集樹變成如何？（請直接繪出結果）

9. (10%) 一正整數若恰好等於除了它自身之外所有因數的和，則該整數被稱為完美數(perfect number)。例如：正整數 6 的因數（但不含 6 本身）有 1、2、3 而 1+2+3=6，因此 6 是完美數。另以正整數 8 為例，因 1+2+4≠8，故 8 不是完美數。試以 pseudo-code 或任何合乎語法的程式語言來描述一程式，判斷自 10 到 10000 的數字範圍中的完美數有哪些，並能將這些完美數顯示於適當的輸出裝置上。

10. (10%) 試以 pseudo-code 或任何合乎語法的程式語言來描述一程式，該程式以遞迴呼叫的方式能將給定的十進位數轉為其對應的 N 進位數（N 可為超過 10 的任意正整數）。例如：若給定的十進位數為 58 而 N 為 12，則輸出 4A。

國立雲林科技大學
98學年度碩士班入學招生考試試題

系所：電機系
科目：電子學

1. In GaAs, the mobilities are μ_n=8500cm^2/V-s and μ_p=400cm^2/V-s.
   (a) Determine the range in conductivity for a range in donor concentration of $10^{15} \leqq N_d \leqq 10^{19}$cm^{-3}. (5%)
   (b) Using the result of part (a) determine the range in drift current density if the applied electric field is E=0.1V/cm. (5%)

2. The secondary voltage in the circuit in Figure 1 is $v_s = 24\sin\omega t$ V, where f = 60Hz. Zener diode has parameters V_Z = 16V at I_Z = 40 mA and r_z = 2.0 Ω.
   (a) Determine R_l such that the load current can vary over
   40 ≦ I_L ≦ 400m A with $I_{Z(min)}$ = 40 mA. (5%)
   (b) Find C such that the ripple voltage is no larger than 1.0 V. (5%)

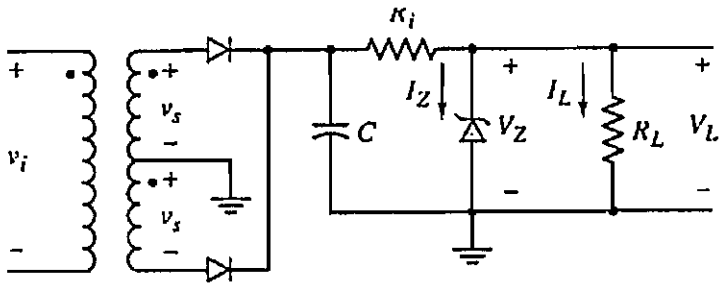


Figure 1

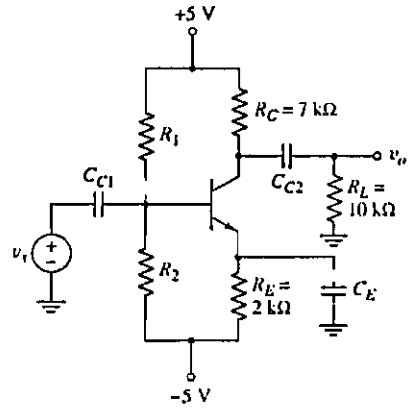


Figure 2

3. Design R_1 and R_2 to achieve maximum symmetrical swing in the output voltage and to maintain a bias-stable circuit shown in Figure 2. The total instantaneous C-E voltages is to remain in the range $1.0 \leqq v_{CE}$ and the total instantaneous collector current is to be $i_C \geqq 0.1mA$. (Note: β=100, $V_{BE(on)}$=0.7V and V_A=∞) (15%)

4. The parameters of the transistor in the circuit in Figure 3 are β=150 and V_A=∞.
   (a) Determine R_1 and R_2 to obtain a bias-stable circuit with the Q-point in the center of the load line. (10%)
   (b) Determine the small-signal voltage gain A_v= v_o/v_s. (5%)

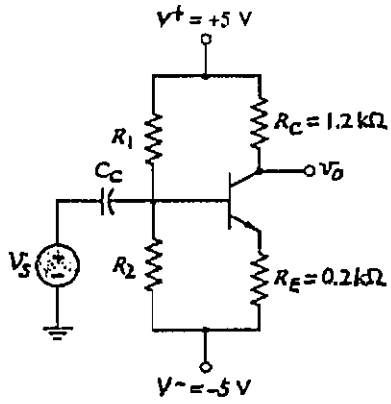


Figure 3

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5. For the PMOS common-source amplifier with a source degeneration resistor and a load capacitor are shown in Figure 4. The parameters are : V_{DD} = +5V, V_{SS} = -5V, R_G = 200kΩ, R_S = 3.2kΩ, R_D = 10kΩ, R_L = 20kΩ, C_L = 10pF, $\frac{1}{2}\mu_p C_{ox}\frac{W}{L}$ = 0.25mA/V^2, V_{TP} = -2V, $\lambda = 0$.

   (a) Perform DC analysis and find I_{DQ}, V_{GSQ}, V_{SDQ}, g_m. (Q represents quiescent point). (8%)

   (b) Draw the small signal equivalent circuit diagram. (5%)

   (c) Calculate the maximum voltage gain $|A_v|_{max}$. (3%)

   (d) Calculate the time constant and the corner frequency. (4%)

6. For the differential MOSFET amplifier shown in Figure 5, the circuit parameters are V_{DD} = +5V, V_{SS} = -5V, R_B = 80kΩ and R_D = 40kΩ. The transistor parameters are V_{TN} = 0.8V, $\lambda = 0$, $\left(\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\right)_{1,2}$ = 0.05mA/V^2, $\left(\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\right)_{3,4}$ = 0.1mA/V^2.

   (a) Calculate the reference current I_{REF}. (5%)

   (b) Determine the quiescent currents of M_1 and M_2. (5%)

   (c) Determine the range of common-mode input voltage. (5%)

   (d) Determine the differential voltage gain $A_d = \frac{v_o}{v_d}$ where $v_o = v_{o2} - v_{o1}$, $v_d = v_1 - v_2$. (5%)

7. Figure 6 depicts a current-to-voltage converter. The current source has a finite output resistance R_S. Assume the parameters of the operational amplifier as the following : (1) The finite open-loop differential gain is A_{od}; (2) The input resistance is infinite; (3) The output resistance is zero.

   (a) Show that the input resistance is given by $R_{in} = \frac{R_F}{1 + A_{od}}$. (5%)

   (b) If R_F = 20kΩ and A_{od} = 1000, determine the range of R_S such that the output voltage deviates from its ideal value by less than 1%. (5%)

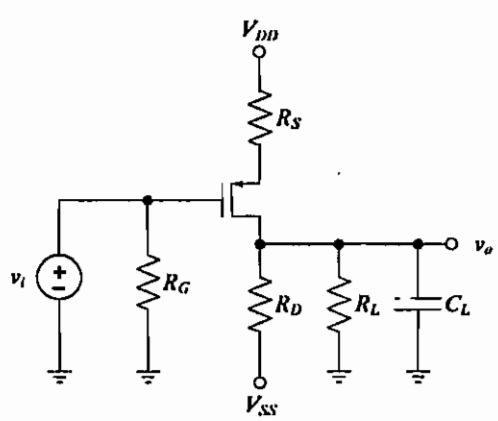

Figure 4

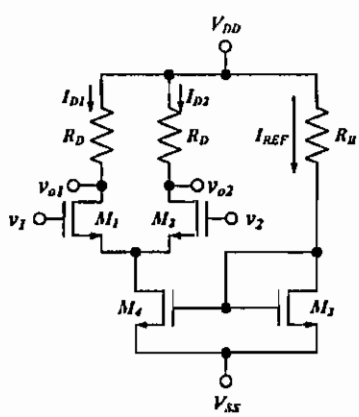

Figure 5

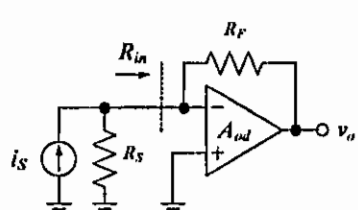

Figure 6