國立雲林科技大學
97學年度碩士班入學招生考試試題

系所：電機系
科目：電路學

1. (20%)

Find the Thevenin equivalent of the circuit to the left of nodes A-B in Fig. 1with k=10 for (a) $R_2=\infty$ and (b) $R_2=50k\Omega$.

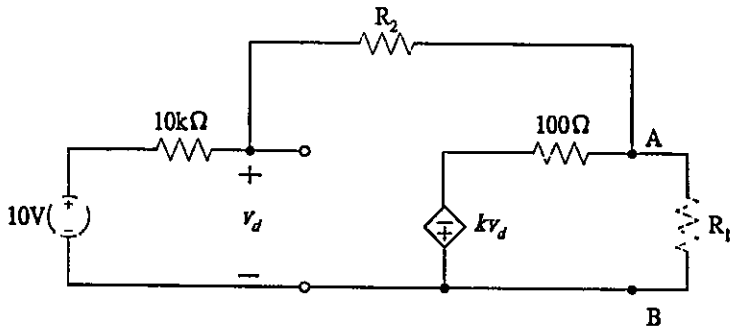

Fig. 1

2. (15%)

For the two-port network shown in Fig. 2 find the values of R_1, R_2, and C, given that the voltage transfer function is

$$H_v(s)=\frac{V_o(s)}{V_i(s)}=\frac{0.2}{s^2+3s+2}$$

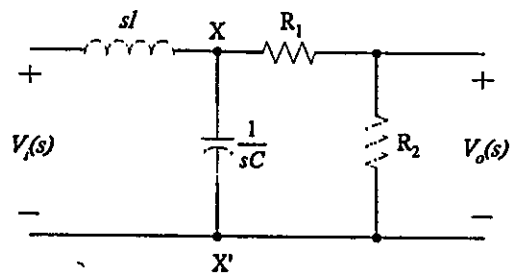

Fig. 2

3. (15%)

For the network in Fig. 3, find the value of the source voltage V which results in $V_o=5\angle 0^\circ$ V.

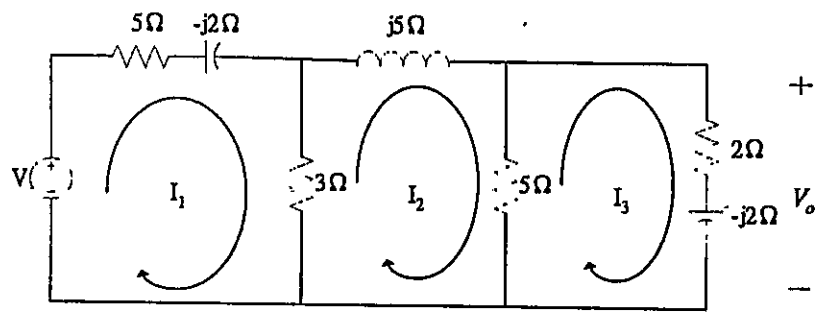

Fig. 3

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系所：電機系
科目：電路學

4. Obtain the complete power triangle for the circuit shown in Fig.4, if the total reactive power is 2500 var (inductive). (7%) Find the branch powers P1 and P2. (8%)

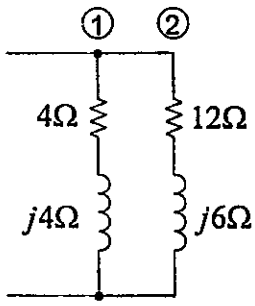

Fig.4

5. Measurements on a practical inductor at 10 MHz give L= 8.0 μH and $Q_{inductor} = 40$. Find the ideal capacitance C for parallel resonance at 10 MHz and calculate the corresponding bandwidth β. (15%)

6. Obtain the dotted equvalent circuit for the coupled circuit shown in Fig.5 (7%), and use it to find the voltage V across the 10Ω capacitive reactance (13%).

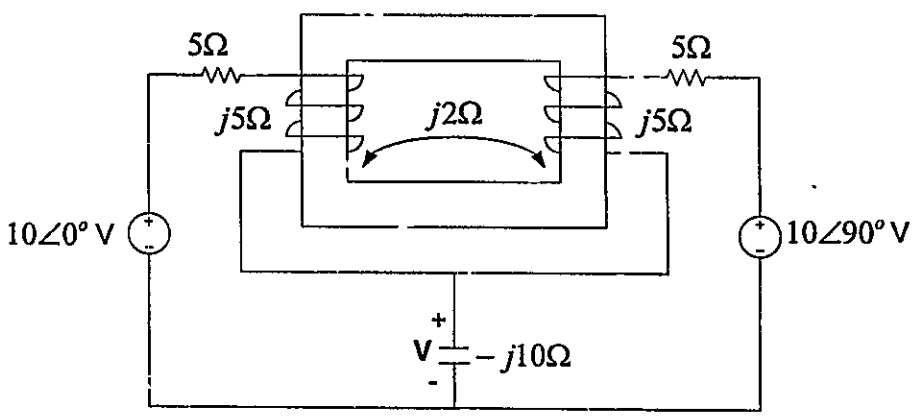

Fig.5

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系所：電機系
科目：資料結構

本試題共9題，共計100分，請依題號作答並將答案寫在答案卷上，
逾者不予計分。

1. (a) (2%) 設計能表示稀疏矩陣（sparse matrix）的資料結構。
   (b) (10%) 繼(a)再設計一個副程式(subroutine)能將一個稀疏矩陣作轉置(transpose)。請以 pseudo-code 或任何合乎語法的程式語言來描述你所設計的副程式。
   (c) (3%) 請討論在(b)所設計的副程式之計算複雜度為何？

2. (8%) 分頁法(paging)可用以管理虛擬記憶體（virtual memory）。然而在程式執行過程中，分頁會逐漸佔據記憶體空間，因而需要適當的分頁替換(page replacement)策略。LRU (Least Recently Used) 替換策略為：當需要選出一個分頁作為「犧牲者」時，選取最久未被使用過的分頁作為即將被置換的對象。請運用堆疊（stack）技術來實現LRU替換策略。請以pseudo-code或任何合乎語法的程式語言來描述你的設計。

3. (a) (5%) 繪出一環形鏈結串列（circularly linked list）的資料結構可表示多項式 $3y^8+2y^5+1$。
   (b) (10%) 說明為何回收一環形鏈結串列所需的時間複雜度僅需 $O(1)$。(以演算法或示意圖方式說明皆可)

4. (a) (9%) 設有二字串欲作模式比對（pattern matching），請描述一套可解決此問題的程序。請以 pseudo-code 或任何合乎語法的程式語言來描述。
   (b) (3%) 請討論在(a)所設計的程序之計算複雜度為何？

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系所：電機系
科目：資料結構

5. 令a，b為兩個正整數。
   (a) (5%) 試以遞迴(recursive)的方式寫出一個程式來找出它們的最大公因數(Greatest Common Divisor, GCD)。請以pseudo-code或C語言(但不可用指標)來描述。
   (b) (5%) 試以$a=1288$，$b=88$為例來說明你的程式之執行步驟。

6. (a) (3%) 在一個圖形中，何謂關鍵節點(articulation point)?
   (b) (3%) 試找出圖1中之所有的關鍵節點。
   (c) (3%) 在一個圖形中，何謂 biconnected component?
   (d) (3%) 試找出圖1中之所有的 biconnected components。

7. (8%) 給定一棵非空的二元樹(nonempty binary tree) T。令n_0是分支度(degree)為0之節點的數目，n_2是分支度為2之節點的數目，試証明$n_0=n_2+1$。

8. (a) (5%) 選擇一個雜湊函數(hash function)應該考慮哪些因素?
   (b) (5%) 給定一組鍵值(key values) 18，22，13，11，21，9，16。試將這7個鍵值利用下列的雜湊函數$h(k)$放入含有 10 個位置的位址空間(從0到9)，若產生碰撞(collision)情況，請將產生碰撞的鍵值列出。
   $h(k)= k^2 \bmod 10$，此處mod為模數(modulus)運算，k為鍵值。

9. (a) (6%) 試設計一個拓樸排序(topological sorting)演算法。請以pseudo-code或C語言來描述。
   (b) (4%) 給定一個有向圖，如圖2所示，試依你的演算法列出其中一組可能的拓樸排序結果。

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系所：電機系
科目：資料結構

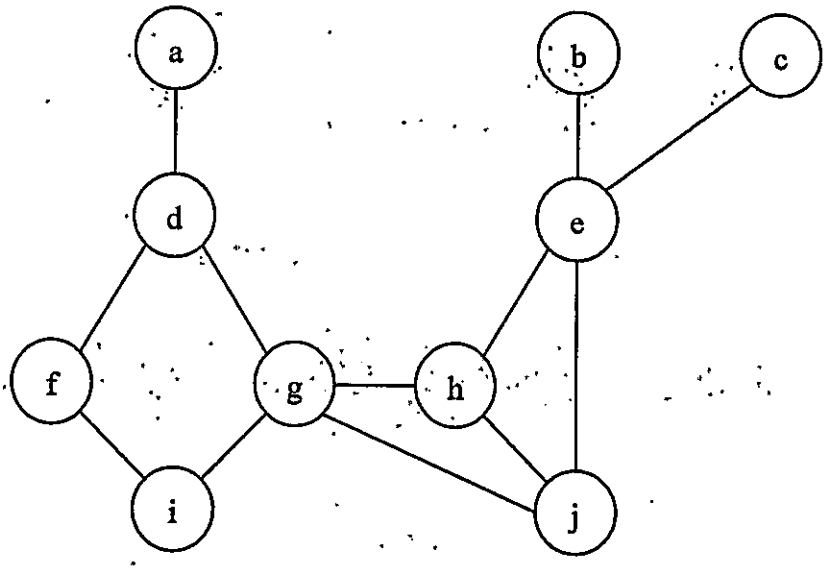

圖 1

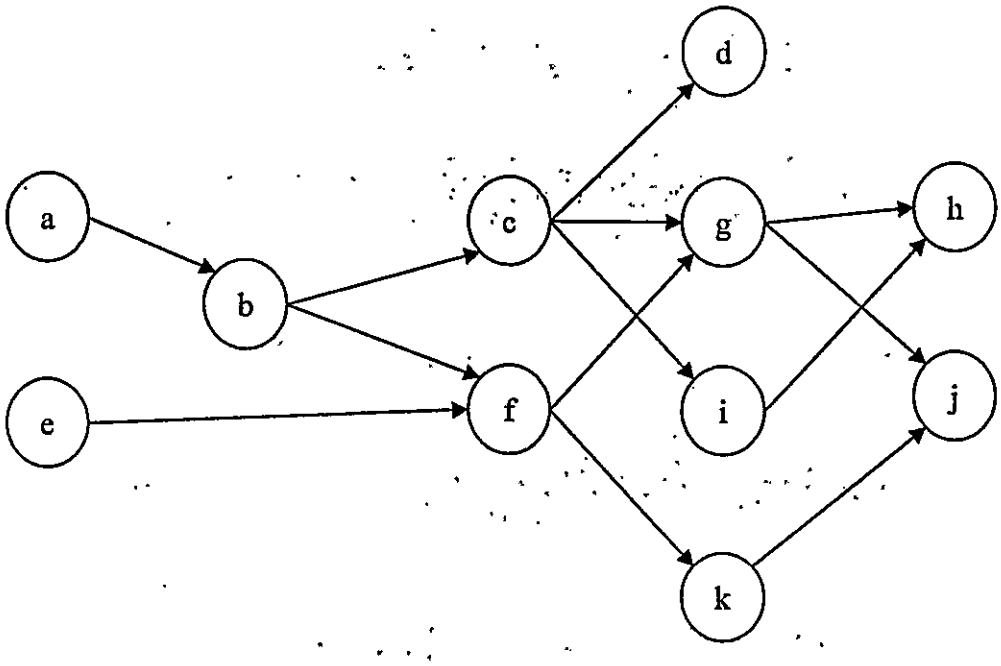

圖 2

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97學年度碩士班入學招生考試試題

系所：電機系
科目：電力系統

1. The voltage $v(t) = 141.4\cos\omega t$ V is applied to a load consisting of a 10Ω resistor in parallel with an inductive reactance $X_L = \omega L = 3.77\Omega$. Calculate the instantaneous power absorbed by the resistor and by the inductor. Also calculate the real and reactive power absorbed by the load, and the power factor. (20%)

2. Three single-phase two-winding transformers, each rated 400MVA, 13.8/199.2kV, with leakage reactance X_{eq}=0.1 per unit, are connected to form a three-phase bank. Winding resistances and exciting current are neglected. The high-voltage windings are connected in Y. A three-phase load operating under balanced positive-sequence conditions on the high-voltage side absorbs 1000MVA at 0.9p.f. lagging, with $V_{AN} = 199.2\angle 0^o$ kV. Determine the voltage V_{an} at the low-voltage bus if the low-voltage windings are connected (a) in Y, (b) in Δ. (30%)

3. Given the symmetrical components to be $V_0 = 10\angle 0°$ V, $V_1 = 80\angle 30°$ V, $V_2 = 40\angle -30°$ V compute the unbalanced phase voltages V_a, V_b, and V_c. (10%)

4. An area of an interconnected power system has two fossil-fuel units operating on economic dispatch. The variable operating costs of these units are given by

$$C_1 = 8P_1 + 9\times 10^{-3}P_1^2 \quad \$/hr$$
$$C_2 = 10P_2 + 8\times 10^{-3}P_2^2 \quad \$/hr$$

where P_1 and P_2 are in megawatts. Determine the power output of each unit, the incremental operating cost, and the total operating cost C_T that minimizes C_T as the total load demand P_T = 900 MW. Generating unit inequality constraints and transmission losses are neglected. (20%)

5. A set of nonlinear algebraic equations in matrix format is given by

$$\mathbf{f(x)} = \begin{bmatrix} f_1(\mathbf{x}) \\ f_2(\mathbf{x}) \\ \vdots \\ f_N(\mathbf{x}) \end{bmatrix} = \mathbf{y}$$

where **y** and **x** are N vectors and **f(x)** is an N vector of functions. Given **y** and **f(x)**, we want to solve for **x**. Explain how to solve by the Newton-Raphson method. (20%)

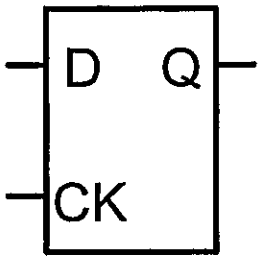
國立雲林科技大學
97學年度碩士班入學招生考試試題

系所：電機系
科目：計算機概論 (丁)

1. (10%) 請將下面的運算式乘開為積項和(Sum of Products)的型式。

   $(W+X+Y')(W'+X'+Z)(W'+Y+Z')(W+Y'+Z)$

2. (10%) 請用下圖的 D 型正反器(D-Flip/Flop)設計一個負緣觸發(Negative Edge Trigger)的四位元位移暫存器(Shit-Register)。(可以視需要加入其它邏輯閘)



圖一

3. (5%) (a)請使用四個雙輸入反及閘(NAND)來設計具有時脈(CK)輸入的的 SR 拴鎖(Latch)。
   (5%) (b)請寫出此 SR 拴鎖電路的真值表。

4. 請寫出下列縮寫的英文全名並解釋其中文意義：
   (4%) (a) BIOS
   (4%) (b) DMA
   (4%) (c) CPU

5. (4%) (a) 請寫出四位元 Gray-Code 碼與十進位數字的對照表。
   (4%) (b) 請以文字解釋 Gray-Code 碼的特性。

國立雲林科技大學
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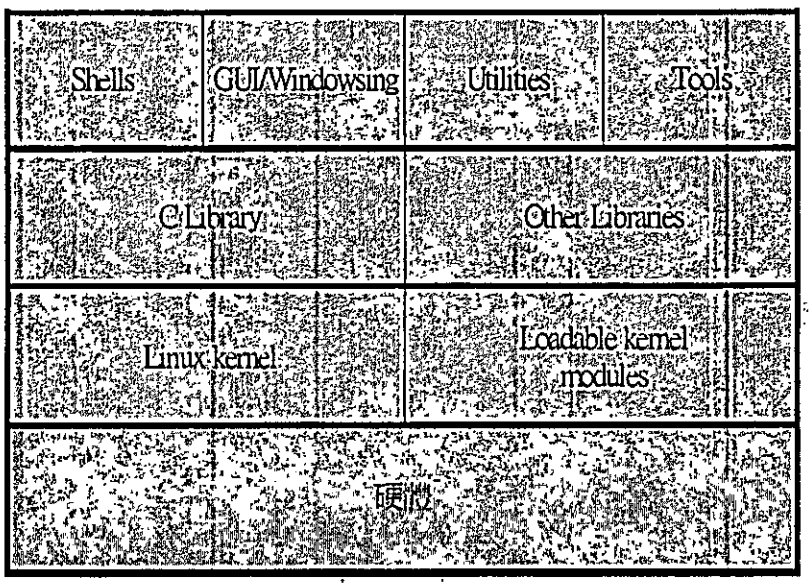
系所：電機系
科目：計算機概論 (丁)

6. Embedded Linux 作業系統之建置是基於現成的 Linux 作業系統。請說明 Linux 作業系統與 Embedded Linux 作業系統的差異性？請參考圖二的作業系統架構圖做說明：
   (a) (5%)Linux 與 Embedded Linux 所使用的硬體平台(Hardware platform)有何差異？
   (b) (5%)Linux 與 Embedded Linux 所採用的系統核心(Linux kernel)與可載入核心模組(Loadable kernel modules)有何差異？



圖二

7. 一般處理器的組合語言指令集(Assembly Instruction Set)，可以分成精簡指令集(RISC)與複雜指令集(CISC)，二大類。請問：
   (a) (5%)請問精簡指令集(RISC)型的處理器有何優點？有何缺點？
   (b) (5%)為何精簡指令集(RISC)型的處理器比較常被嵌入式系統領域所採用？

8. 為何 Java 程式語言(Java Language)與 Java 虛擬機器(Java Virtual Machine)，特別適合應用於嵌入式系統的應用軟體開發工作？請從以下 Java 技術所具備的五大優點特色來分析：
   (a) (2%)物件導向特性(Object oriented)？
   (b) (2%)可攜性(Portability)？
   (c) (2%)自動回收記憶體管理(Garbage collection)？
   (d) (2%)支援網路處理能力(Network layer support)？
   (e) (2%)動態載入程式庫(Dynamic loading Java classes)？

9. 程式設計如圖三。假設 p 變數所在的記憶體位址為：0x22ff74，且 ptr1 變數所在的記憶體位址為：0x22ff70：
   (a)（4%）*ptr1 =？
   (b)（4%）ptr1=？

(c) (4%) **ptr2 = ?

(d) (4%) *ptr2 = ?

(e) (4%) ptr2 = ?

```
#include <iostream>
using namespace std;
int main() {
    int p = 10;
    int *ptr1 = &p;
    int **ptr2 = &ptr1;
    return 0;
}
```

圖三

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系所：電機系
科目：自動控制

1. Solve for $y(t)$ for the following system represented in state space, where $u(t)$ is the unit step. Uses the Laplace transform approach to solve the state equation (15%)

$$\dot{X}=\begin{bmatrix}-3 & 1 & 0\\ 0 & -6 & 1\\ 0 & 0 & -5\end{bmatrix}X+\begin{bmatrix}0\\ 1\\ 1\end{bmatrix}u(t)$$

$$y=[0 \quad 1 \quad 1]X;\ X(0)=\begin{bmatrix}0\\ 0\\ 0\end{bmatrix}$$

2. Using Mason's rule, find the transfer function, $T(s)=C(s)/R(s)$, for the system represented in Figure 1. (10%)

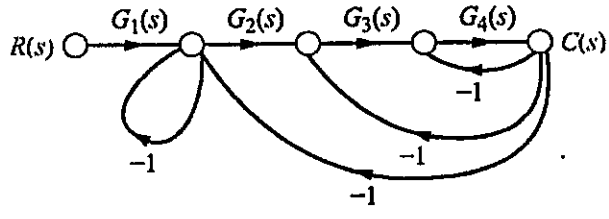

Figure 1

3. Given the system (15%)

$$\dot{X}=\begin{bmatrix}0 & 3 & 1\\ 2 & 8 & 1\\ -10 & -5 & -2\end{bmatrix}X+\begin{bmatrix}10\\ 0\\ 10\end{bmatrix}u(t)$$

$$y=[0 \quad 1 \quad 1]X$$

Find out how many poles are in the left half-plane, in the right half-plane, and on the $j\omega$-axis.

4. Find the sensitivity of the steady-state error to changes in parameter K and parameter a for the system shown in Figure 2 with a step input. (10%)

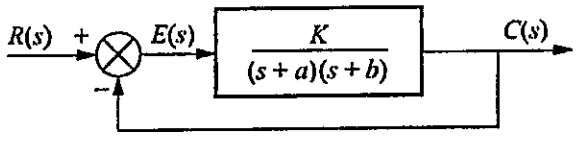

Figure 2

國立雲林科技大學
97學年度碩士班入學招生考試試題

系所：電機系
科目：自動控制

5. Given a unity feedback system that has the forward path transfer function:

$$G(s)=\frac{K}{(s+4)(s^2+2s+2)}$$

Find the root locus for the following terms: (20%)

(a) Departure angle . (10%)

(b) Range of K for stability. (10%)

6. . Consider the system with the transfer function (20%)

$$g(s)=\frac{2s+1}{s^3+s^2+s-6}$$

(a) Find the controllable canonical form of the system (A_c, B_c, C_c)

(b) Design a feedback controller, K so that the poles of the closed-loop are assigned at s =-5, -3 ± j3.

7. Plot the Nyquist diagram for the unity feedback system with the open-loop transfer function, (10%)

$$G(s)=\frac{500}{(s+1)(s+3)(s+10)}$$

國立雲林科技大學
97學年度碩士班入學招生考試試題

系所：電機系
科目：工程數學

1. Find the general solution of the differential equation (10 分)

$\left[D^3-2D^2+D\right]y=2x;$ [Note: $D^n y=y^{(n)}=\frac{d^n}{dx^n}y$]

2. Find the general solution, $y(x)=c_1y_1(x)+c_2y_2(x)$, of the differential equation $x^2y''+xy'-y=0,\quad x>0$. To explain if y_1, y_2 are linear independent by Wronskain test. (15 分)

3. Let $A=\begin{bmatrix}-1 & 0\\ 1 & -5\end{bmatrix}$, find: (1) P, and diagonal matrix $D=P^{-1}AP$,
(2) $(A^2+6A+4I)^5=?$ (10 分)

4. To solve the initial value problem, $\begin{matrix}x_1'=2x_1-10x_2\\ x_2'=-x_1-x_2\end{matrix}$, $X(0)=\begin{bmatrix}7\\0\end{bmatrix}$, by matrix methods。(15 分)

5. Find the Laplace transform for the following functions (10%)
$[\sin(t-1)+(t^2-2)]H(t-1)$

6. Find the inverse Laplace transform for the following functions.

(a) $\ln[(s+2)/(s-1)]$, (10%)

(b) $\frac{se^{-2s}}{(s+2)^2(s^2+4s+8)}$. (10%)

7. Find the sum of the series $\sum_{n=1}^{\infty}(-1)^n/(4n^2-1)$. (hint :expand sin(x) in a Fourier cosine series on [0 π] and choose an appropriate value of x. (10%)

8. Find the inverse Fourier transform for function: $\frac{2e^{(\omega-2)i}}{[2+(\omega-2)i]}$. (10%)

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系所：電機系
科目：電子學

1. In the circuit in Fig.1 with transistor parameters $\beta = 180$ and $V_A = \infty$, design the bias resistors R_1 and R_2 to achieve maximum symmetrical swing in the output voltage and to maintain a bias-stable circuit. The total instantaneous C-E voltage is to remain in the range $0.5 \le v_{CE} \le 4.5\,\text{V}$ and the total instantaneous collector current is to be $i_C \ge 025\,\text{mA}$. ($R_1 // R_2 = 1.81k\Omega$) (25%)

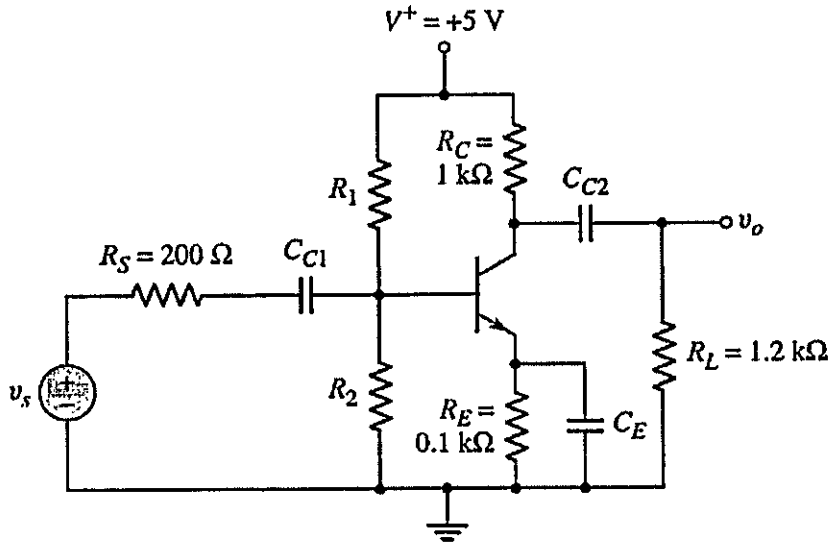

Fig.1

2. For the circuit shown in Fig.2, the transistor parameters are: $I_{DSS} = 6mA$, $|V_p| = 2V$, and $\lambda = 0$. (a) Calculate the quiescent drain current and source-to-drain voltage of Q1 (10%) (b) Derive the expression of the overall small-signal voltage gain. (15%)

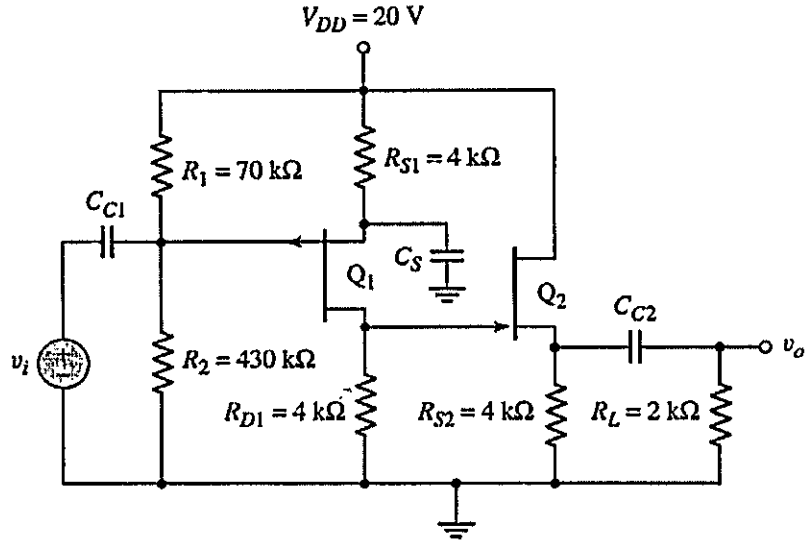

Fig.2

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系所：電機系
科目：電子學

3. For the MOSFET circuit shown in Fig. 3, the transistor parameters are : $\frac{1}{2}\mu_n C_{ox}\frac{W}{L}=1\text{mA/V}^2$, V_{TN}=1V, $\lambda=0$, $C_{gs}=2\text{pF}$, $C_{gd}=0.5\text{pF}$.
   (a) Calculate I_D, g_m. (5%)
   (b) Draw the simplified high-frequency equivalent circuit. (5%)
   (c) Find the midband voltage gain. (5%)
   (d) Calculate the equivalent Miller Capacitance. (5%)
   (e) Determine the upper 3dB frequency for the small-signal voltage gain. (5%)

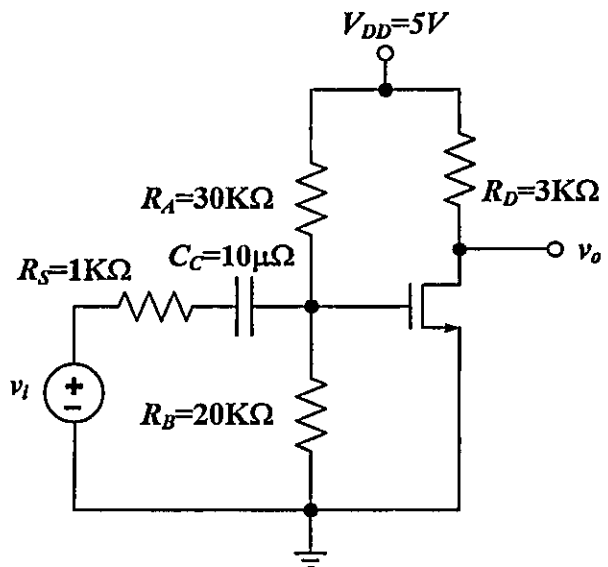

Figure 3

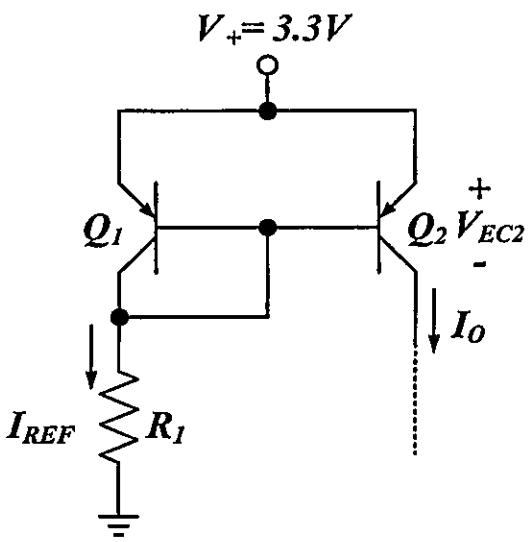

Figure 4

4. Figure 4 shows a basic two-transistor pnp current source. The transistor parameters are : $\beta=50$, $V_{EB}(\text{on})=0.6\text{V}$, and $V_A=50\text{V}$. The transistor value of R_1 is designed at 9KΩ. Determine I_O for (a) $V_{EC2}=0.6\text{V}$, (b) $V_{EC2}=2\text{V}$. (10%)

5. Consider a four pole feedback loop system with a loop gain given by

$$T(f)=\frac{\beta(10^4)}{\left(1+j\frac{f}{10^6}\right)\left(1+j\frac{f}{10^7}\right)\left(1+j\frac{f}{10^8}\right)\left(1+j\frac{f}{10^9}\right)}$$

Determine the value of β and the frequency that produces a phase margin of 45 degrees. (15%)

國立雲林科技大學
97學年度碩士班入學招生考試試題

系所：通訊所、電機系
科目：線性代數

1. (10%) Let $\mathbf{u}$ be a vector in $\mathbf{R}^2$ whose projection onto the $x-axis$ is u_x as shown in Figure 1. Determine the entries of the vector $\mathbf{u}$.

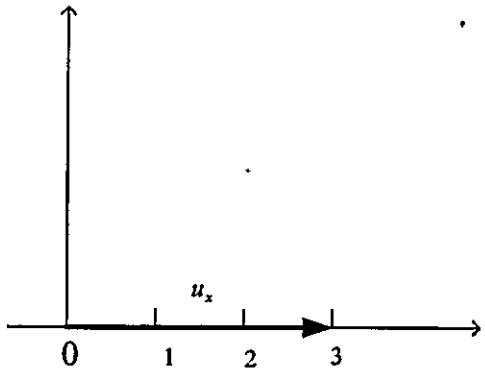

Figure 1.

2. (10%) Let

$$\mathbf{A} = \begin{bmatrix} 6 & 2 & 8 \\ 9 & 5 & 11 \\ 3 & 1 & 6 \end{bmatrix}$$

$$\mathbf{L} = \begin{bmatrix} 2 & 0 & 0 \\ t & s & 0 \\ 1 & 0 & -1 \end{bmatrix}$$

$$\mathbf{U} = \begin{bmatrix} r & 1 & 4 \\ 0 & 2 & -1 \\ 0 & 0 & p \end{bmatrix}$$

Find scalars r, s, t and p so that $\mathbf{LU} = \mathbf{A}$.

3. (15%) Determine whether each of the following statements is *True* or *False*, and explain.

(a) $\det(A+B) = \det(A) + \det(B)$

(b) $\det\left(A^{-1}B\right) = \frac{\det(B)}{\det(A)}$

(c) If $\det(A) = 0$, then A has at least two equal rows.

(d) If A has a column of all zeros, then $\det(A) = 0$.

(e) A is singular if and only if $\det(A) = 0$.

4. (15%) Let

$$S = \left\{ \begin{bmatrix} 1 \\ 2 \\ 0 \end{bmatrix}, \begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix}, \begin{bmatrix} 2 \\ 8 \\ -2 \end{bmatrix}, \begin{bmatrix} 3 \\ 0 \\ 0 \end{bmatrix}, \begin{bmatrix} 4 \\ 0 \\ 1 \end{bmatrix} \right\}.$$

Show that $span(S) = \mathbf{R}^3$ and find a basis for $\mathbf{R}^3$ consisting of vectors from S.

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5. (15%) Let $L: \mathbf{R}^3 \rightarrow \mathbf{R}^3$ be a linear transformation for which we know that

$$L\left(\begin{bmatrix}1\\0\\1\end{bmatrix}\right)=\begin{bmatrix}1\\2\\3\end{bmatrix},\quad L\left(\begin{bmatrix}0\\1\\2\end{bmatrix}\right)=\begin{bmatrix}1\\0\\0\end{bmatrix}, L\left(\begin{bmatrix}1\\1\\0\end{bmatrix}\right)=\begin{bmatrix}1\\0\\1\end{bmatrix}$$

(a) Find $L\left(\begin{bmatrix}4\\1\\0\end{bmatrix}\right)=?$

(b) Find $L\left(\begin{bmatrix}0\\0\\0\end{bmatrix}\right)=?$

6. (10%) Consider vector space $\mathbf{R}^2$.

(a) For what values of m and b will the set of all vectors of the form $\begin{bmatrix}x\\mx+b\end{bmatrix}$ be a *subspace* of $\mathbf{R}^2$?

(b) For what value of r will the set of all vectors of the form $\begin{bmatrix}x\\rx^2\end{bmatrix}$ be a *subspace* of $\mathbf{R}^2$?

7. (10%) Let L: $\mathbf{R}^2 \rightarrow \mathbf{R}^2$ be the linear transformation defined by

$$L\left(\begin{bmatrix}x_1\\x_2\end{bmatrix}\right)=\begin{bmatrix}x_2-x_1\\2x_1+x_2\end{bmatrix},$$

and let

$$S = \left\{\begin{bmatrix}1\\0\end{bmatrix},\begin{bmatrix}0\\1\end{bmatrix}\right\}$$
$$T = \left\{\begin{bmatrix}1\\1\end{bmatrix},\begin{bmatrix}2\\1\end{bmatrix}\right\}$$

be two bases for $\mathbf{R}^2$. Find the matrix representation $[L]_T^S$ of L with respect to T and S.

8. (15%) Let $A=\begin{bmatrix}3&1\\0&2\end{bmatrix}$.

(a) Find a nonsingular matrix P such that $P^{-1}AP$ is diagonal.

(b) Derive a formula for A^k, where k is any positive integer.

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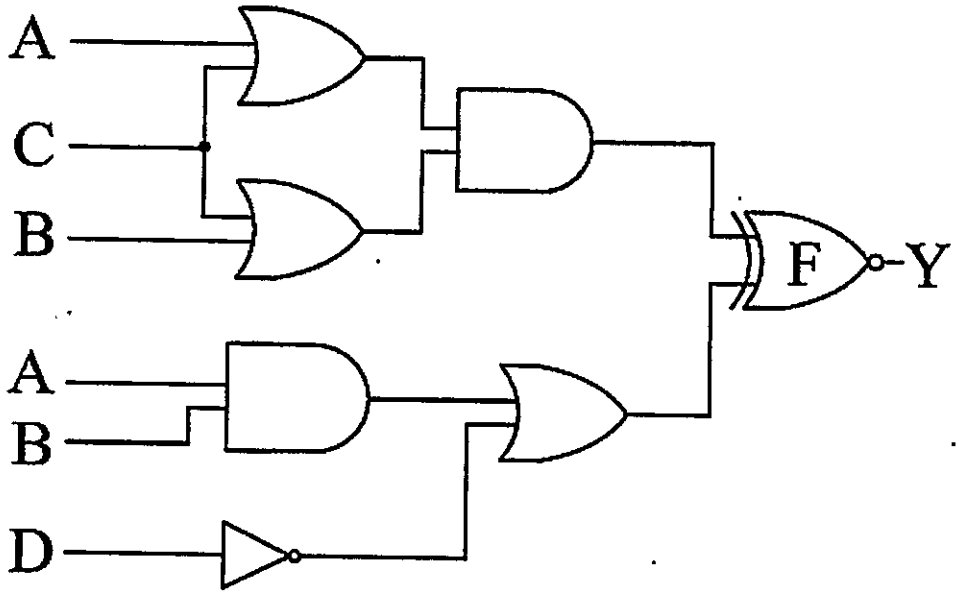
本試題共十題，每題 10 分，共計 100 分，請依題號作答並將答案寫在答案卷上，違者不予計分。

1. 有一個邏輯電路，設計如圖一：
   (a) (5%)請說明 F 邏輯閘是哪一種邏輯閘？邏輯運算符號為何？
   (b) (5%)用卡諾圖(Karnaugh Map)化簡方法求出 Y 布林函數的 minimum sum of product？



圖一

2. 請比較以下二種加法器的架構與缺點：
   (a) (5%)請用圖解的方式說明連波進位加法器(Ripple-Carry Adder)的架構與原理？其缺點為何？
   (b) (5%)請用圖解的方式說明前瞻進位加法器(Carry-Lookahead Adder)的架構與原理？其缺點為何？

3. 任何的布林代數函數都可以用 NOT, OR, AND,三種基本邏輯閘來實現。因此，任何的邏輯電路模組如果可以實現上述三種基本邏輯閘，就可以實現任何的布林代數函數：
   (a) (4%)請用圖解的方式說明 4-to-1 多工器電路模組可以實現 NOT 基本邏輯閘？
   (b) (3%)請用圖解的方式說明 4-to-1 多工器電路模組可以實現 OR 基本邏輯閘？
   (c) (3%)請用圖解的方式說明 4-to-1 多工器電路模組可以實現 AND 基本邏輯閘？

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4. 假設某個處理器有三類指令集，分別是指令集A、指令集B及指令集C。而且，各個指令集的單位指令執行時間(Cycles Per Instruction, CPI)分別為 CPI_A, CPI_B, CPI_C。
   (a) (5%)當處理器的時脈頻率被調高到原來的110%時，而指令集A、指令集B及指令集C的單位指令執行時間(Cycles Per Instruction, CPI) CPI_A, CPI_B, CPI_C都沒有任何變動。請問此處理器的效能增益(Performance Gain)為何？效能增益(Performance Gain)的定義如下：
   Performance Gain = (Original Overall Processing Time / New Overall Processing Time) – 100%
   (b) (5%)當處理器的時脈頻率被調高到原來的120%時，而 $CPI_{A'} = 1.2CPI_A$, $CPI_{B'}=CPI_B$(不變), $CPI_{C'}=CPI_C$(不變)。假如指令集A佔整個運算過程中的40%，而指令集指令集B與指令集C佔整個運算過程中的60%，請問此處理器的效能增益(Performance Gain)為何？

5. 一般處理器的組合語言指令集(Assembly Instruction Set)，可以分成精簡指令集(RISC)與複雜指令集(CISC)，二大類。請問：
   (a) (5%)請問精簡指令集(RISC)型的處理器有何優點？有何缺點？
   (b) (5%)為何精簡指令集(RISC)型的處理器比較常被嵌入式系統領域所採用？

6. (a) (3%) 何謂多核心（multiple compute cores）處理器？
   (b) (7%) 有哪些方法可讓多核心處理器益加發揮效能？

7. 考慮圖二所示之C語言程式。令每個整數型態資料均佔用4位元組（bytes）記憶體空間。

```
#include <stdio.h>

void main ()
{
   int i, j, num[3][3] = {0};
   int **ptr1 = &num[2];
   int *ptr2 = &num[0][0];

   for (i = 0; i < 3; i++)
      for (j = 0; j <= i; j++) num[i][j] = (i+1)*(j+1);
   *(ptr2+4) = -1;
   printf("%d, %d\n",*ptr1, *(ptr2+8));
}
```

圖二

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(a) (5%) 圖二程式的 printf() 輸出結果為何？
(b) (5%) 圖二程式在即將執行 printf() 之時，num 陣列中的元素值分別為何？(須寫出所有正確的元數值才給分)

8. (a) (5%) 試說明計算機系統中的中斷處理（interrupt handling）流程。
(b) (5%) 請以計時器（timer）中斷為例，說明服務該中斷的流程。

9. (a) (3%) 何謂 P2P（peer-to-peer）技術？
(b) (7%) 使用 P2P 軟體有何缺點？

10. (a) (5%) 請說明「線路交換」（circuit switching）及「分封交換」（packet switching）技術的工作方式。
(b) (5%) 比較「線路交換」與「分封交換」之不同點。